EDV-9500

OPERATION MANUAL

US Model

BCS 37488

ED Beta

711B2 CHASSIS

MICROFILM

Beta

ED BETA VIDEO CASSETTE RECORDER

SONY

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1. VIDEO CIRCUIT

1-1. INPUT/OUTPUT (I/O) CIRCUIT

1-1-1. Y Signal Input

(When a video input)

The video signal input from the video input terminal passes through the S video input and Y signal changeover switch IC001 and then passes through the input switch IC003 and AGC circuit IC004 and is input to the Y/C separation comb filter where Y/C separation is carried out. However, if the input signal is black and white (B/W) (when there is no burst signal), it is input directly to the Y comb filter without passing through the Y/C separation comb filter similar to the Y signal input. Furthermore, the tuner video signal is selected by IC003.

(When an S image input)

The Y signal input from the S image input terminal passes through the image input video signal changeover switch IC001 and is input to the Y comb filter of the VI board after passing through the input changeover switch IC003 and the AGC circuit IC004.

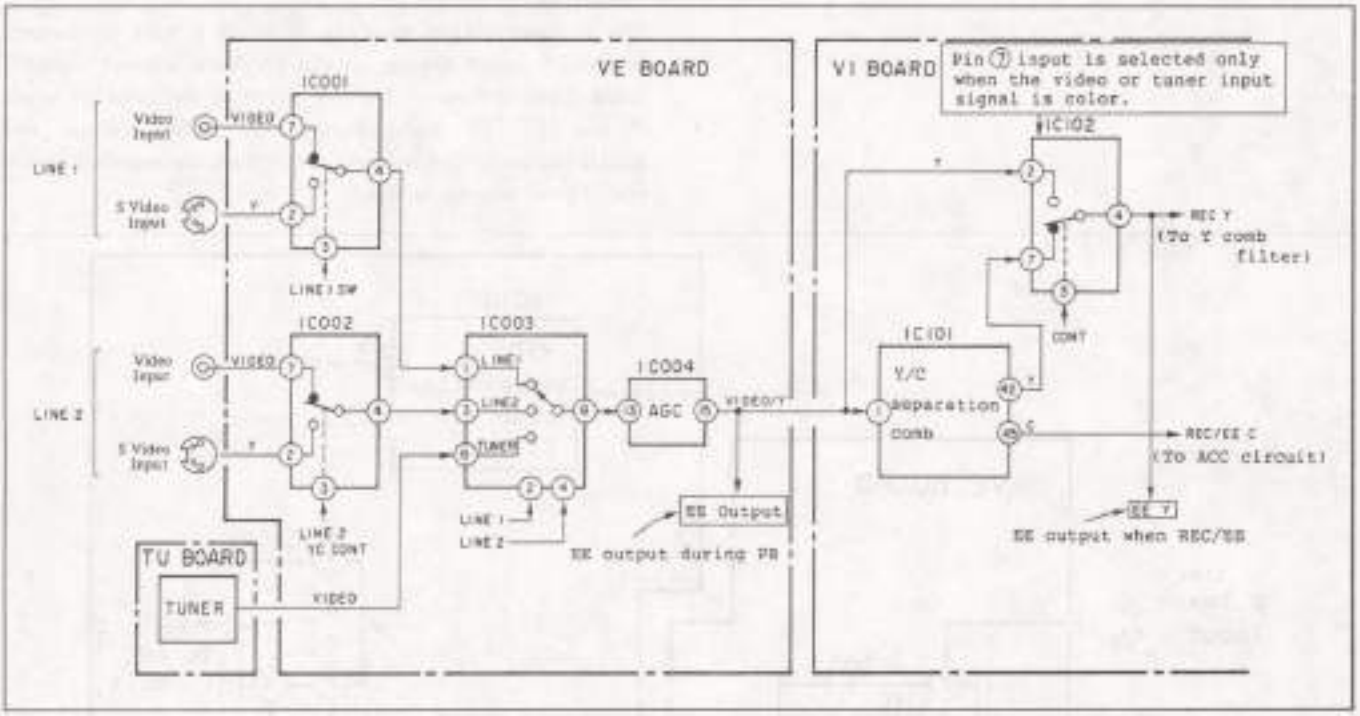


Fig. 1-1

1-1-2. Chroma Signal Input

(When a video input)

The chroma signal on which Y/C separation was carried out by IC101 of the VI board is input to the ACC circuit.

(When an S image input)

The chroma signal input to the S image input terminal is input to the ACC circuit of the VI board after passing through input switch IC200.

1-1-3. S Image Output

(When REC/EE)

The Y signal is branched in the VI board before entering the Y comb filter and is then input to the VE board. The Y signal passes through IC601 and 004 where character signals are mixed in and is then output from the S image output terminal. The chroma signal that passed through the ACC circuit is also branched in the VI board and is input to the VE board. This chroma signal passes through IC602 and 201 where blanking is conducted on the character-inserted portion and is output to the S image output terminal.

In the digital picture mode (stop motion/flash motion), the output signal of the VI board is input to the DI board where digital picture processing is carried out and it is then input to the VE board. This signal switching is carried out in IC601 and 602 of the VE board by switching signal SWMM. The SWMM signal is a signal output from the memory controller of the DI board and becomes "L" in the digital picture mode and the variable speed PB mode.

(When PB)

The playback output from the VI board is input unchanged to the VE board during normal playback without variable speed. Current flow in the VE board is the same as when in the REC/EE mode. Signals that passed through the digital picture circuit are output in variable speed playback and digital picture modes.

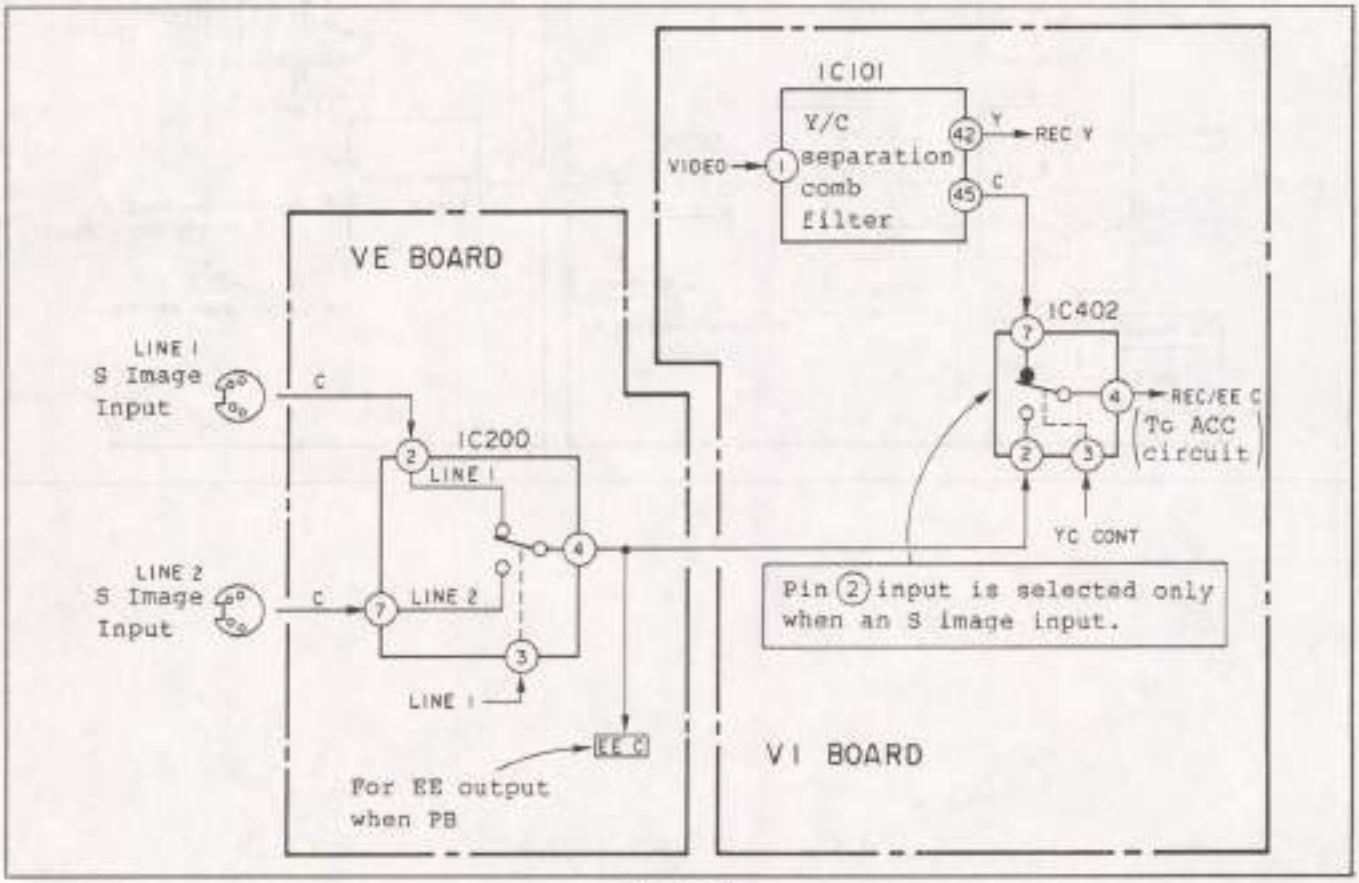


Fig. 1-2

The following signals are also output when the EE button is pressed.

- In the case of a video input (including tuner input)
  The video signal output of the AGC circuit (Pin ⑱ of IC004) passes through the 3.58 MHz trap and becomes the Y signal. It also passes through the 3.58 MHz BPF and becomes the chroma signal. The two signals are selected respectively in IC004 and IC201 and become the Y signal output and chroma signal output.
- In the case of an S image input
  The Y signal output from the AGC circuit (Pin ⑲ of IC004) passes through the 3.58 MHz trap and becomes the Y signal output after being selected by IC004.
  The chroma signal selected in input switch IC200 is selected by IC201 and becomes the chroma output.

1-1-4. Video Output

The video output signal is created by mixing the chroma signal and Y signal for S image output in the YX-1 board (IC500).
After its chroma spectrum components are removed in the comb filter, the Y signal is mixed with the chroma signal to prevent cross colors.

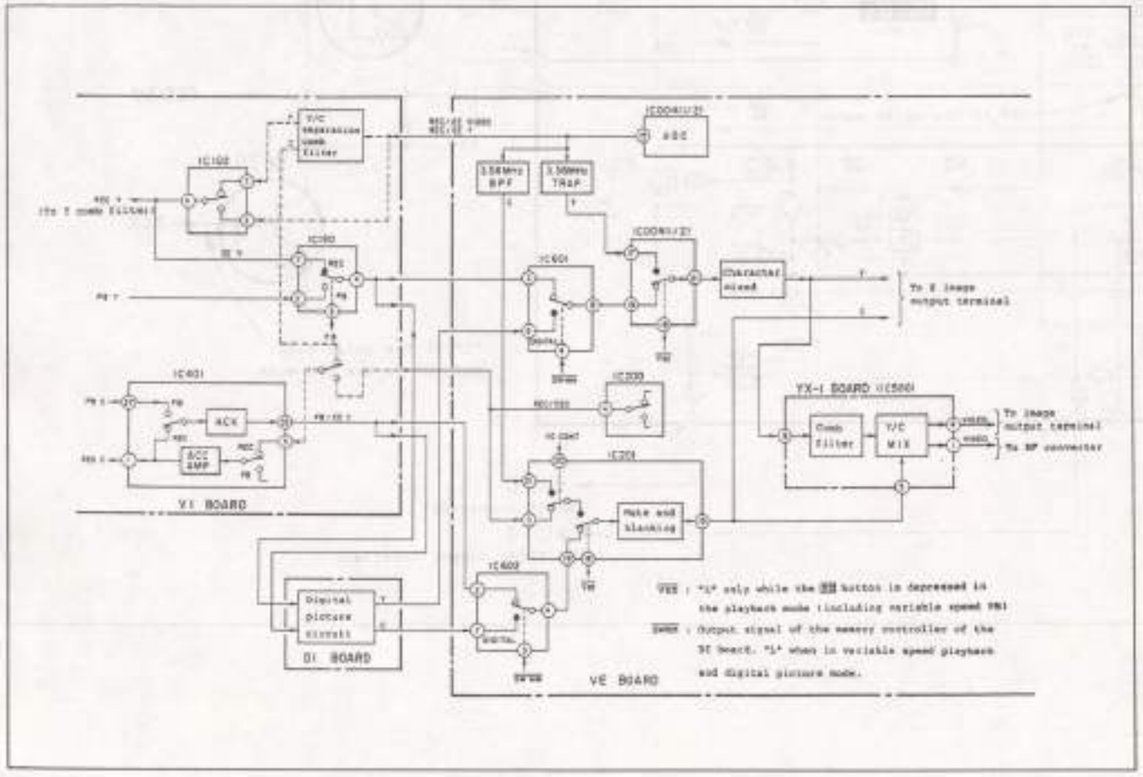


Fig. 1-3

1-1-5. 3.58 MHz Comb Filter

Since the playback frequency band of ED Beta is wide, beat will be caused by the effects of jitter if Y/C is mixed directly as in the past.

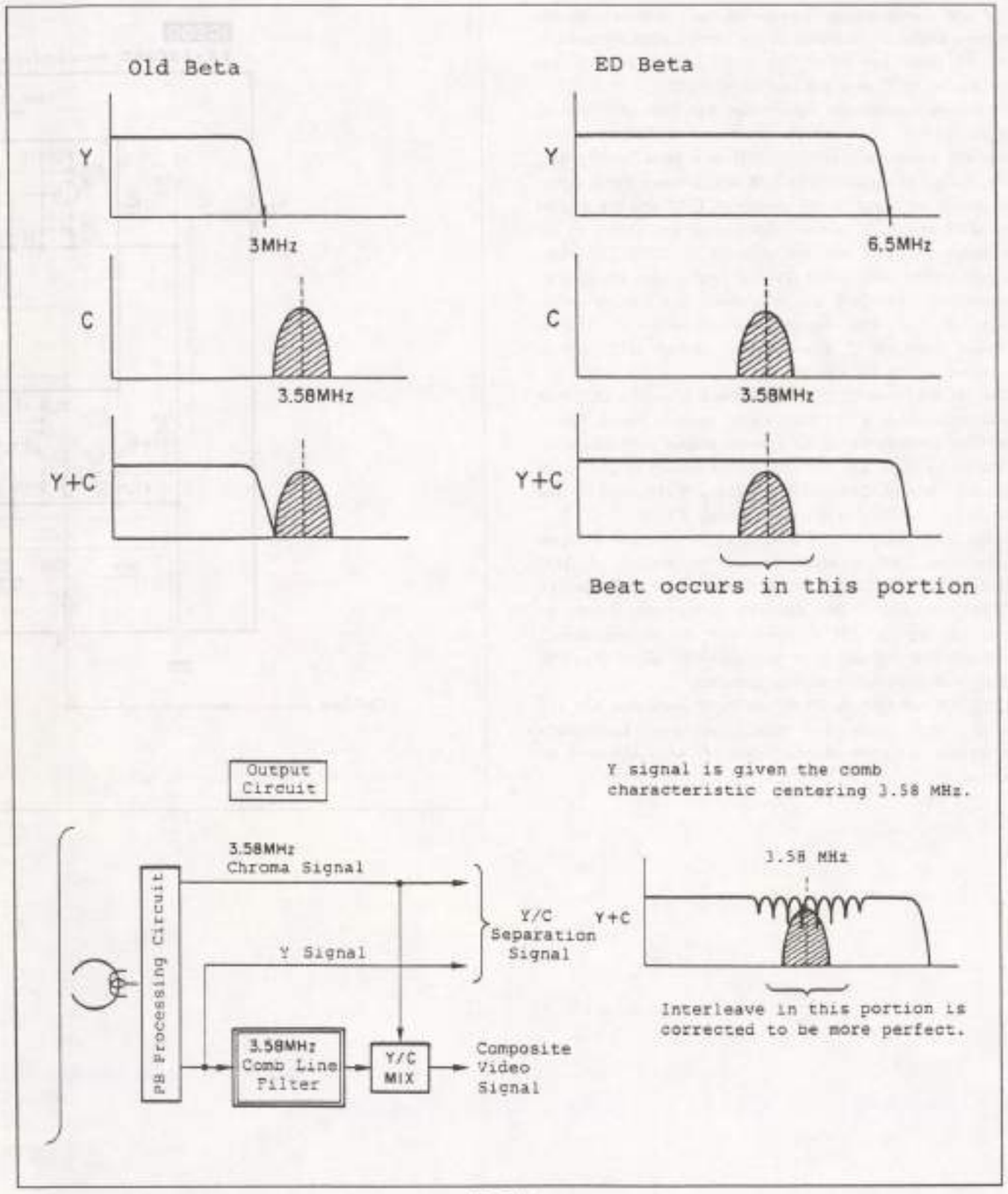


Fig. 1-4

Actual Circuit

The Y signal is input to Pin ⑨ of the YX-1 board, This Y signal is separated into 3.58 MHz component and frequency components other than 3.58 MHz by L101 and C103. The 3.58 MHz frequency component is amplified by Q101 and 102 and the spectrum components that interfere with the chroma signal are removed in the chrome filter centered on the 1H delay line IC101, The signal is then input to the emitter of Q107 and the emitter of Q109,

Frequency components other than 3.58 MHz are input to the emitter of Q107 and the emitter of Q109 after passing through buffer amp Q106.(FL1011 is a band limiting LPF for audio FM signals) The 3.58 MHz chroma signal inputs of Pin ⑤ are input to the emitter of Q107 and the emitter of Q109 and Y/C mixed video signals are output to the collector of Q107 and the collector of Q109. The video signal on the collector of Q107 is output from Pin ④ after passing through Q108 and is supplied to the video output terminal. The video signal on the collector of Q109 is output from Pin ① after passing through Q110 and is supplied to the RF converter,

The 1H delay line (IC101) of the comb filter is a CCD type and the clock is a 10.7 MHz signal input to Pin ⑬. The 3.58 MHz components of the Y signal output of Q102 are 1H delayed by IC101 and are input to the emitter of Q107 after passing through Q104, LPF, Q105 and RV101, and to the emitter of Q109 after passing through RV102.

Aside from this, the 3.58 MHz component of the Y signal output of Q102 is input directly the emitter of Q107 through R107 and C105, and to the emitter of Q109 through C122 and R134. The spectrum components (such as spectrum signals that interfere with the chroma signal) without line correlation of the 3.58 MHz signal input to Q107 and Q109 are therefore cancelled.

Q103, 026 and 027 go ON in the B/W mode and kills the comb filter. This also causes spectrum components interfering with the chroma signal of the Y signal to be output.

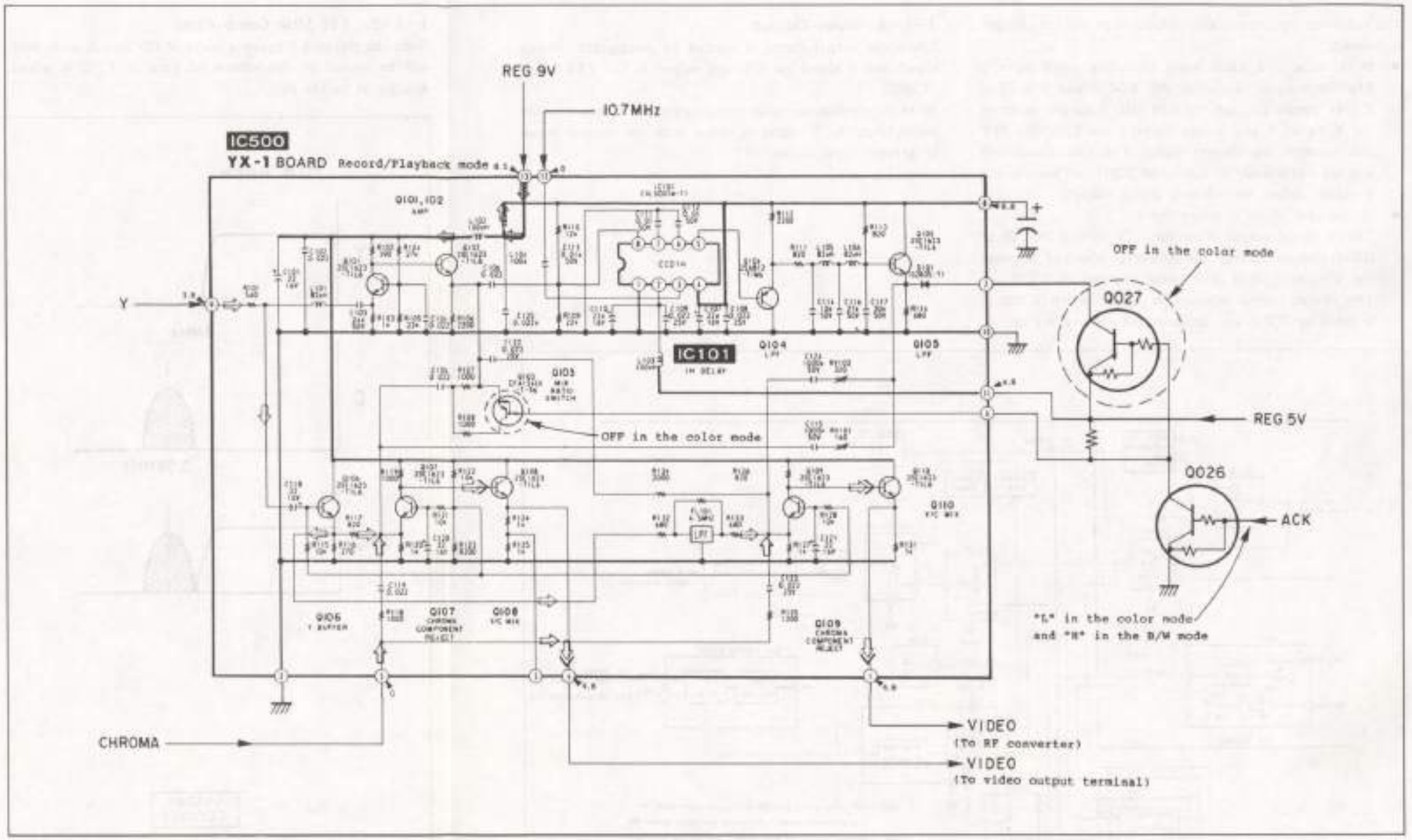


Fig. 1-5

1-2. Y SIGNAL RECORDING SYSTEM

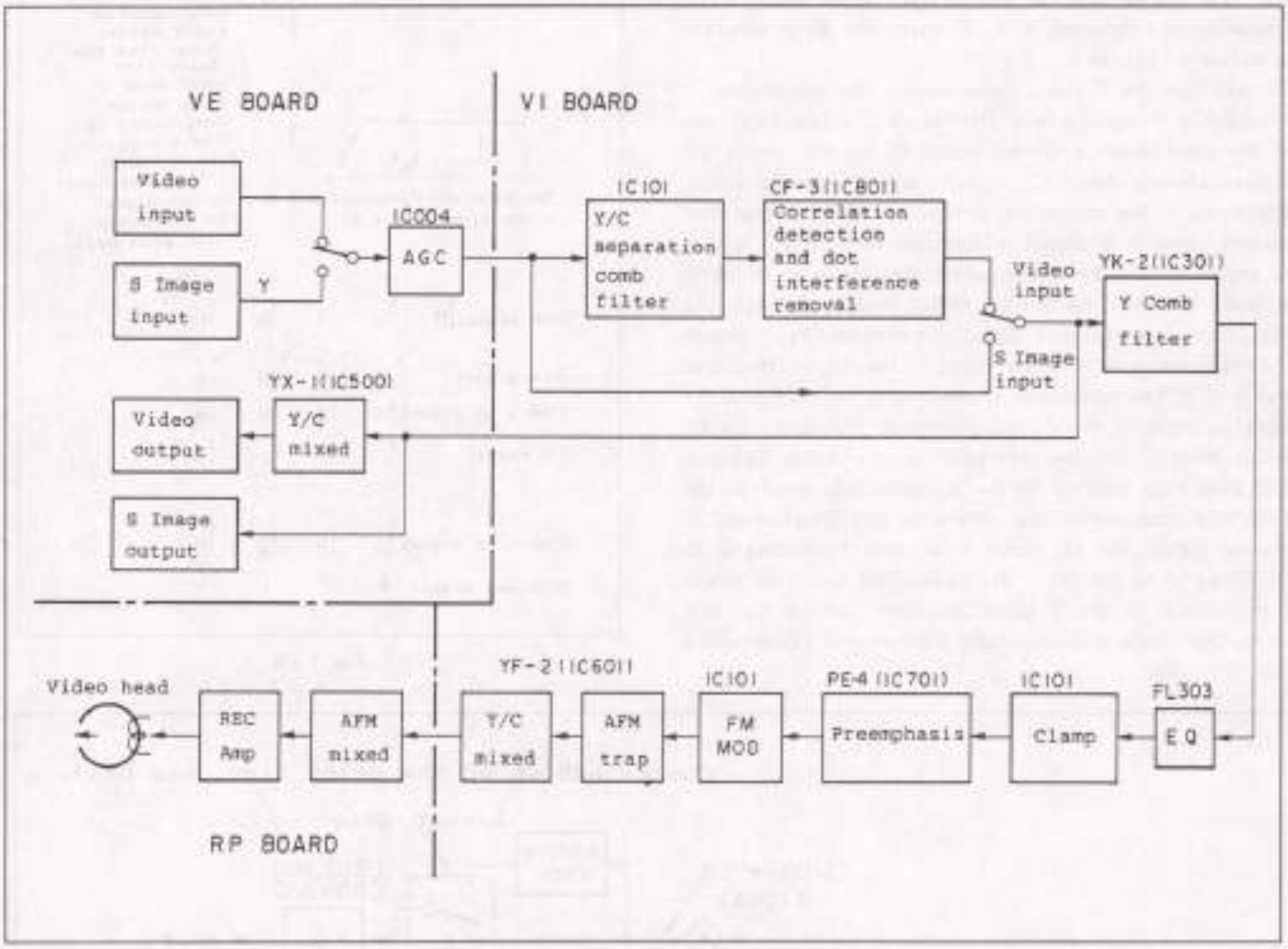


Fig. 1-6

1-2-1. AGC Circuit

Sync AGC and peak AGC processing is initially conducted in IC004 on both video input signals and Y input signals (S image input signal).

The sync AGC detects the sync tip level and pedestal level and controls the gain of the AGC amp so the sync signal level is constant. Burst signals at the pedestal part of the video signal will therefore become a hindrance in detecting. A signal from which chroma signal has been removed in an LPF and chroma trap is therefore input to Pin ㉘.

The peak AGC operates only when the output level of Pin ㉙ exceeds 1.075 Vp-p even if the sync AGC is operating and prevents signal outputs above this level.

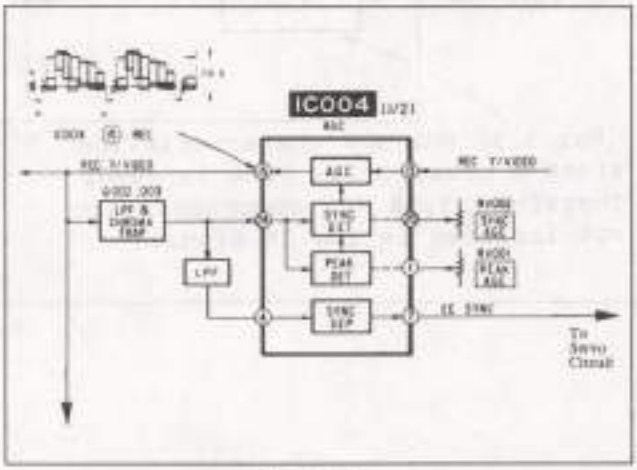


Fig. 1-7

1-2-2. Y/C Separation Circuit

The video signal is input to the comb filter where Y/C separation is conducted. A Y/C separation block diagram is shown in Fig. 1-8.

We will consider a video signal having line correlation. Although a Y signal and a 1H delayed Y signal (Y_D) are of the same phase, a chroma signal (C signal) and a 1H delayed chroma signal (C_D signal) are of opposite phase. Therefore, if the separation process of the Y signal and chroma signal is displayed in spectrum form it will appear as shown in Fig. 1-9. The output signal 0H + 1H of ⓒ is input to the Y comb filter (YK-2 Board) through EQ. Also, since low region Y signal components (Y_L) outside the delay line pass band are mixed in the 0H − 1H output signal of ⓒ, this component is removed in the BPF and the signal is input to the chroma process IC (Pin ⑮ of IC401). When there is no line correlation in the video signal, a 3.58 MHz trap inserted in the Y signal side removes the 3.58 MHz components and eliminates dot interference. In chroma signals, the 1H signal is cancelled by adding a 0H + 1H signal to the 0H − 1H signal. This therefore means that removal of the Y signal is carried out by the BPF alone. Color runs and cross color are removed by cancelling the 1H signal.

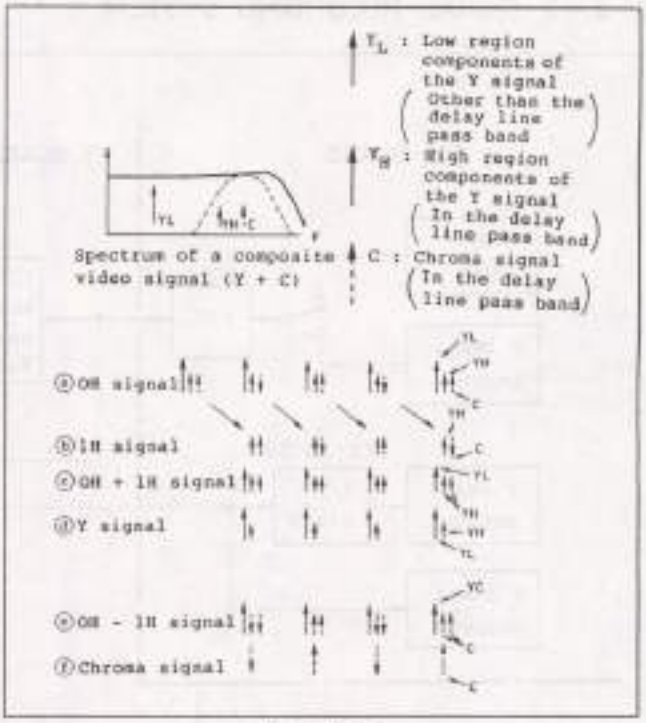


Fig. 1-9

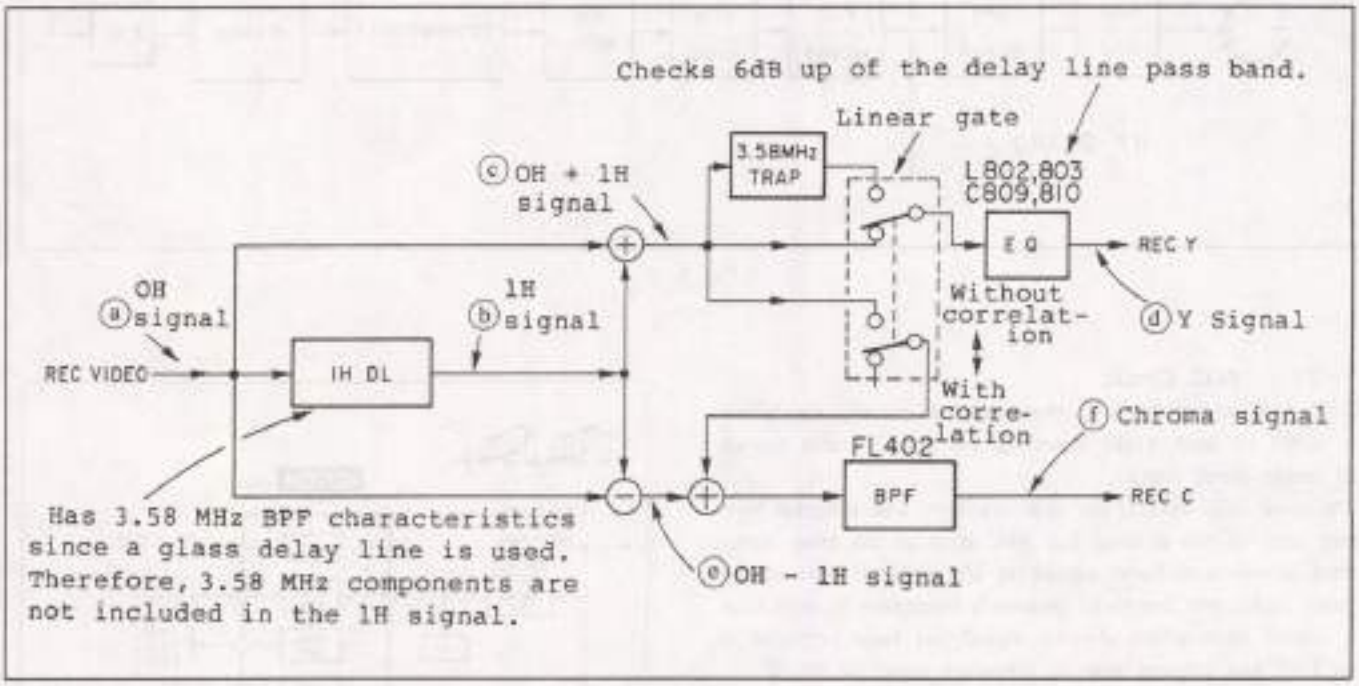


Fig. 1-8

1-2-3. Correlation Detection Circuit

With conventional Y/C separation comb filters using 1H delay line, dot interference or cross color and color runs occur in the part without line correlation.

- Color runs : The chroma signal is displaced downward in relation to the Y signal on the screen.
- Cross color : 3.58 MHz Y signal mixed in with the chroma signal.
- Dot interference : Chroma signals mix in with the Y signal and become dots (3.58 MHz).

In this model, correlation is detected with a 3-line comb filter and cross color and dot interference are removed to prevent the above.

As may be discerned in Fig. 1-10, if we compare the video signal that is not delayed (0H signal) and the 2H delayed video signal (2H signal), the chroma signal and Y signal are of the same phase in the portion with line correlation. Therefore, if we consider the difference between the two signals (2H − 0H signal), the amplitude of this difference signal will be 0 when there is line correlation between the chroma signal and Y signal, and will not be 0 if there is no correlation. In other words, it is possible to detect chroma signal line correlation and Y signal line correlation simultaneously by detecting the amplitude of the 2H − 0H signal.

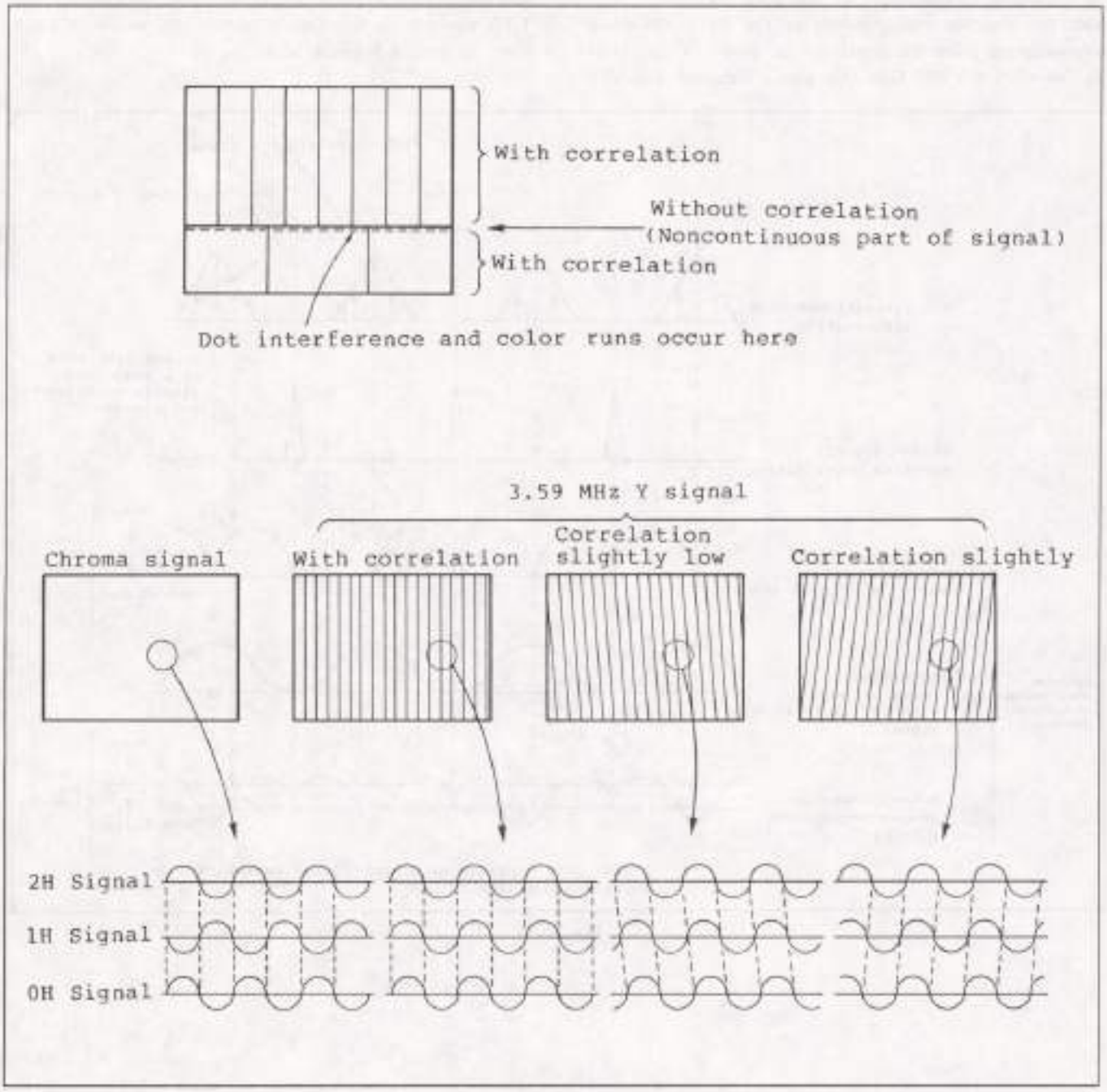


Fig. 1-10

By inserting a 3.58 MHz trap for the Y signal in the output of the Y/C separation comb filter, it will be possible to eliminate dot interference as a result of this detection. Also, color runs and cross color are eliminated by adding the Y signal (actually the 0H + 1H signal) of the Y/C separation comb filter output to the chroma signal (actually the 0H − 1H signal) of the Y/C separation comb filter on the chroma signal side and thus cancelling the 1H delay portion (1H signal).

In actual switching, switching is not merely by means of a switch but is by changing the degree of cancellation of the 1H delay signal (chroma signal side) or the depth of the 3.58 MHz trap (on the Y signal side) smoothly corresponding to correlation of the input signal.

Also, the detection characteristics by the 2H − 0H signal become sharp comb characteristics as shown in Fig. 1−11 Ⓐ. Therefore, the 3.58 MHz trap also affects the 3.58 MHz Y signal with its slightly low line correlation as shown in Fig. 1−10. To prevent this, the 0H + 2.1H + 2H signal level is also detected and the detected voltage is subtracted from the voltage of the 2H − 0H signal voltage detected and the detected characteristics corrected as shown in Fig. 1−11 Ⓒ.

Although the Y/C separation comb filter is used to remove chroma signal crosstalk during playback, since color runs will occur if comb filtering is carried out in portions without line correlation in this case, the linear gate is used to cancel the 1H signal as when recording. The Y-YD signal is used to detect correlation in this case since false detection is prone to occur with the 2H − 0H signal because of the chroma signal crosstalk component. The Y-YD signal level detection is carried out by the Y comb filter of the YK-2 board (IC301).

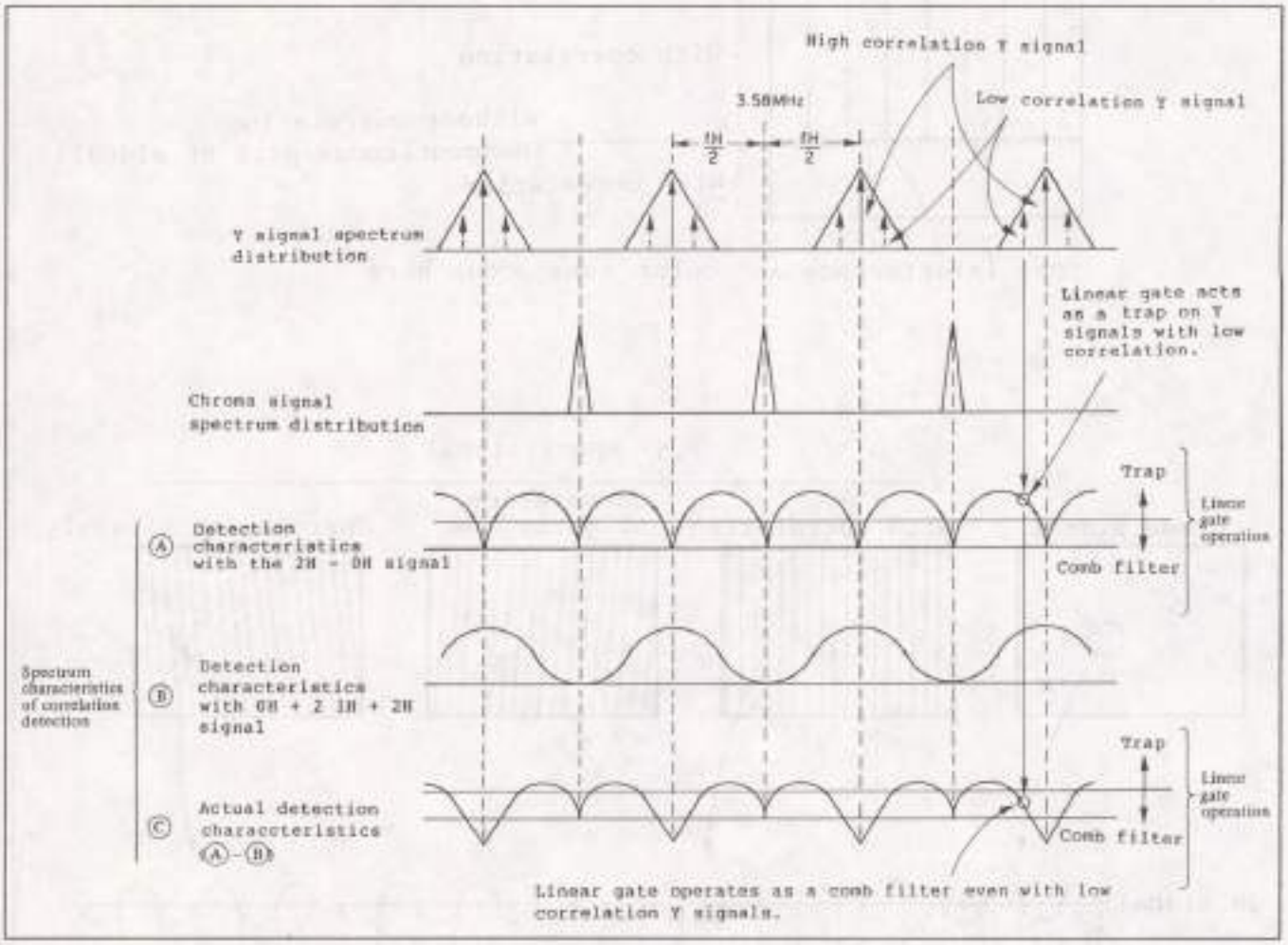


Fig. 1−11

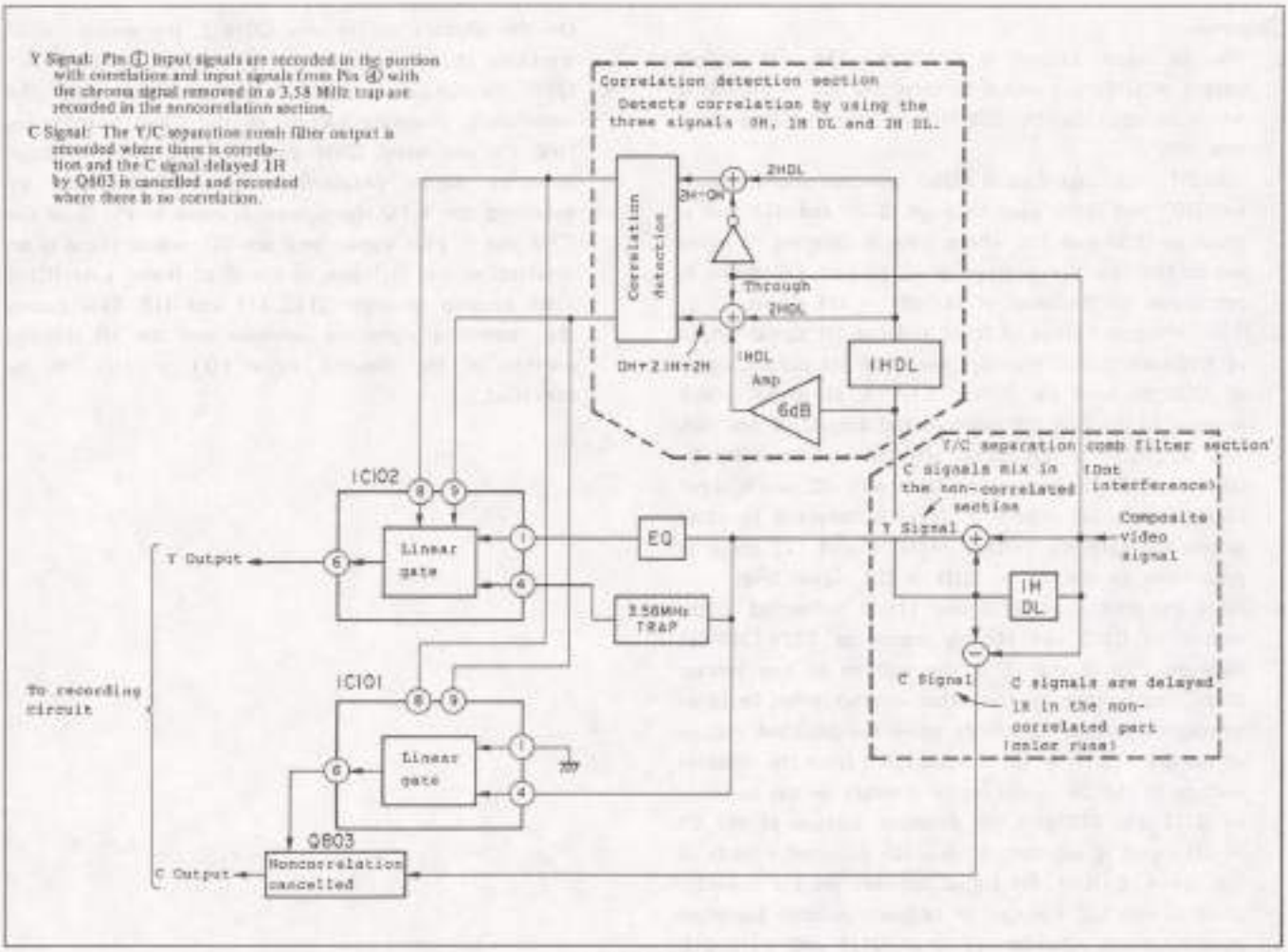

Y Signal: Pin ① input signals are recorded in the portion with correlation and input signals from Pin ④ with the chroma signal removed in a 3.58 MHz trap are recorded in the noncorrelation section.
C Signal: The Y/C separation comb filter output is recorded where there is correlation and the C signal delayed 1H by Q803 is cancelled and recorded where there is no correlation.
Correlation detection section
Detects correlation by using the three signals 0H, 1H DL and 2H DL.
Correlation detection
2H-0H
2HDL
Through
2HDL
0H+2.1H+2H
1HDL Amp
6dB
1HDL
Y/C separation comb filter section
C signals mix in the non-correlated section (Dot interference)
Y Signal
Composite video signal
1H DL
C Signal
C signals are delayed 1H in the non-correlated part (color rusa)
IC102
Linear gate
EQ
3.58MHz TRAP
Y Output
IC101
Linear gate
To recording circuit
Q803
Noncorrelation cancelled
C Output

Fig. 1-12

(Operation)

1. The 2H signal output of Q127 and the −0H signal output of Q120 are added to form the 3H − 0H signal which is input to the 3.58 MHz differential amp Q107 and 109.
2. The 2H − 0H signal (3.58 MHz) selected and amplified by Q107 and Q109 pass through Q123 and 124 and is input to Q113 and 115 where level is detected. In other words, the collector voltage of Q113 and 115 drops in proportion to the level of the 2H − 0H signal.
3. The 0H signal output of Q101 and the 1H signal output of Q126 are added together with the 2H output signal of Q127 to form the 0H + 2.1H + 2H signal which is input to the 3.58 MHz differential amp Q106 and 108.
4. The 0H ; 2.1H + 2H signal selected and amplified by Q106 and 108 passes through Q121 and 122 and is input to Q110 and 112 where its level is detected. In other words, the collector voltage of Q110 and 112 drops in proportion to the 0H + 2.1H + 2H signal level.
5. Since the emitter of Q113 and 115 is connected to the emitter of Q110 and 112 by means of R829 (270 Ω) between Pins ⑬ and ⑭, if the voltage of one emitter drops, the voltage of the other emitter rises. In other words, the voltage difference when the detected voltage of the 0H + 2.1H + 2H is subtracted from the detected voltage of the 2H − 0H signal appears on the collector of Q113 and 115, and the detected voltage of the 2H − 0H signal is subtracted from the detected voltage of the 0H + 2.1H + 2H signal appears on the collector of Q110 and 112. Voltages of opposite polarity therefore appear on the collectors of Q113, Q115 and Q110, 112. (Q111 and 114 are constant current circuits.)
6. The voltage detected on the collector of Q113 and 115 passes through Q116 and is input from Pin ⑩ of linear gate IC101 and 102. The voltage detected on the collector of Q110 and 112 passes through Q119 and is input to Pin ⑨ of IC101 and 102.
7. In linear gate IC101 and 102, the input to Pin ① will be selected by the bias voltage supplied by RV802 and 806 when there is no signal. Therefore, the signal not passing through the 3.58 MHz trap on the Y signal side (IC102 side) is output from Pin ⑪ while video signals with line correlation are input (when the 2H − 0H signal level is 0). Also, since there will be no signal outputs from Pin ⑤ on the chroma signal side (IC101 side), 1H delayed components will not cancelled.
8. If the 2H − 0H signal level becomes high, the collector voltage of Q113 and 115 drops, and the collector voltage of Q110 and 112 rises in sections where line correlation is low, the voltage on Pin ⑩ of linear gate IC101 and 102 drops and the voltage on Pin ⑨ rises. This causes the input signal of Pin ④ of the linear gate to be output from Pin ⑪ and the output signal of the input signal to Pin ① decreases. That is, the signals passing through the 3.58 MHz trap increases on the Y signal side (IC102) and the signals not passing through the trap decreases.

On the chroma signal side (IC101), the cancel signal increases thus cancelling the 1H delayed components.

9. Q807 to Q810 go ON during playback and the correlation detecting circuit of the CF-3 board goes OFF. On one hand, Q806 goes ON and the correlation detection signal obtained in the YK-2 board by detecting the Y-YG signal level is input to Pin ⑬ of the CF-3 board. This signal becomes "H" where there is no correlation and is input to Pin ⑧ of linear gate IC101 after passing through Q110, 112 and 118. This causes the cancelling signal to increase and the 1H delayed portion of the chroma signal (0H − 1H) to be cancelled.

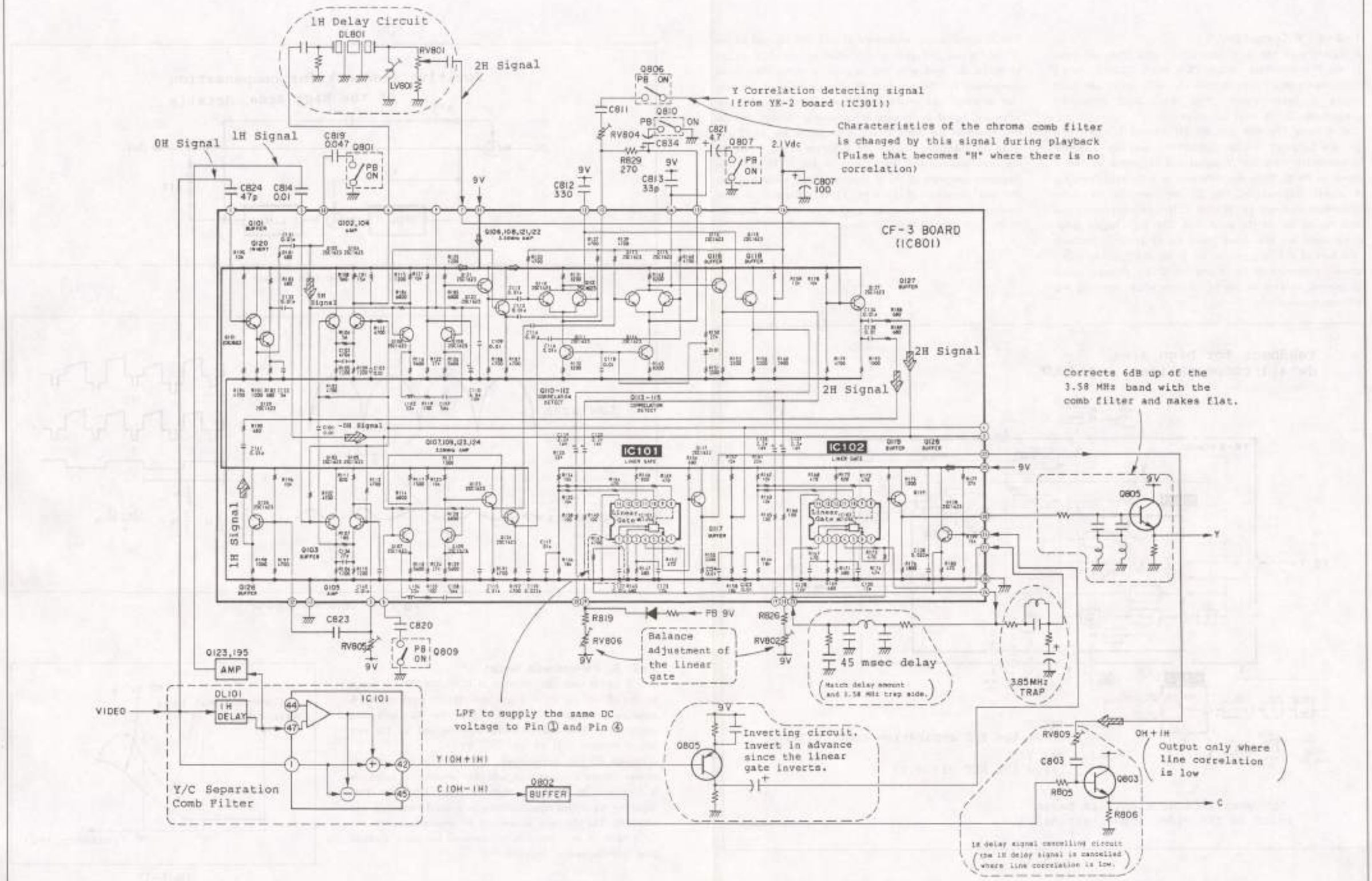

1H Delay Circuit
DL801
RV801
LV801
2H Signal
0H Signal
1H Signal
C819 0.047
Q801
PB ON
C824 47p
C814 0.01
Q806
PB ON
Y Correlation detecting signal
(from YK-2 board (IC301))
C811
Q810
PB ON
RV804
C834
C821 4.7
Q807
PB ON
2.1Vdc
Characteristics of the chroma comb filter is changed by this signal during playback (Pulse that becomes "H" where there is no correlation)
R829 270
9V
C813 33p
C812 330
C807 100
CF-3 BOARD (IC801)
Q101 BUFFER
Q120 INVERT
Q102,104 AMP
Q106,108,121,122 3.58MHz AMP
Q127 BUFFER
Q110-112 CORRELATOR DETECT
Q113-115 CORRELATION DETECT
Q107,109,123,124 3.58MHz AMP
IC101 LINEAR GATE
IC102 LINEAR GATE
Q118 BUFFER
Q126 BUFFER
Q103 BUFFER
Q105 AMP
1H Signal
-0H Signal
C823
C820
RV805
PB ON
Q809
9V
R819
RV806
PB 9V
R826
RV802
Balance adjustment of the linear gate
45 msec delay
(Match delay amount and 3.58 MHz trap side.)
3.85MHz TRAP
Q123,195 AMP
DL101 1H DELAY
IC101
VIDEO
Y/C Separation Comb Filter
Y (0H+1H)
C (0H-1H)
Q802 BUFFER
LPF to supply the same DC voltage to Pin ① and Pin ④
Inverting circuit. Invert in advance since the linear gate inverts.
Q805
Corrects 6dB up of the 3.58 MHz band with the comb filter and makes flat.
RV809
C803
R805
Q803
R806
0H+1H
Output only where line correlation is low
C
1H delay signal cancelling circuit (the 1H delay signal is cancelled where line correlation is low.)

Fig. 1-13

1-2-4. Y Comb Filter

Y signals from the Y/C separation comb filter are input to the Y comb filter of the YK-2 board (IC301) during video inputs and Y signals from the AGC circuit are input during S image inputs. This comb filter principally compensates for H level differences.

The Y signal (Pin ②) and the 1H delayed Y signal (Pin ①) are compared in IC301 (CX-20006B) and the difference is subtracted from the Y signal and is output as the Y signal to Pin ⑫. Since the difference is subtracted from the Y signal obtained on Pin ⑬, not only is the noise component removed but H level difference compensation is also carried out at the same time. The high region detail components are also being corrected by positive feedback of a part of the Y_D signal to the Y signal input. The clamp circuits connected to Pin ① and Pin ② is a pedestal clamp to prevent outputs of the DC portion when detecting the difference component.

The Y signal is AM modulated at 10.7 MHz to add to the 1H DL circuit and gain is controlled by the AGC circuit to match its level with the original Y signal. This is to compensate for the temperature characteristics of the amp that amplifies the modulated wave and the 1H DL line when the signal is detected after passing through the DL line. Assemble the comb filters as shown in Fig. 1-15 and when the characteristics become as shown in Fig. 1-16, the low area becomes the trough part of Fig. 1-16 since the frequency spectrum of the H level difference signal becomes the odd sequence of $1/2\ f_H$. Level difference is then removed and the detail components in the vertical direction of the high area will be reinforced.

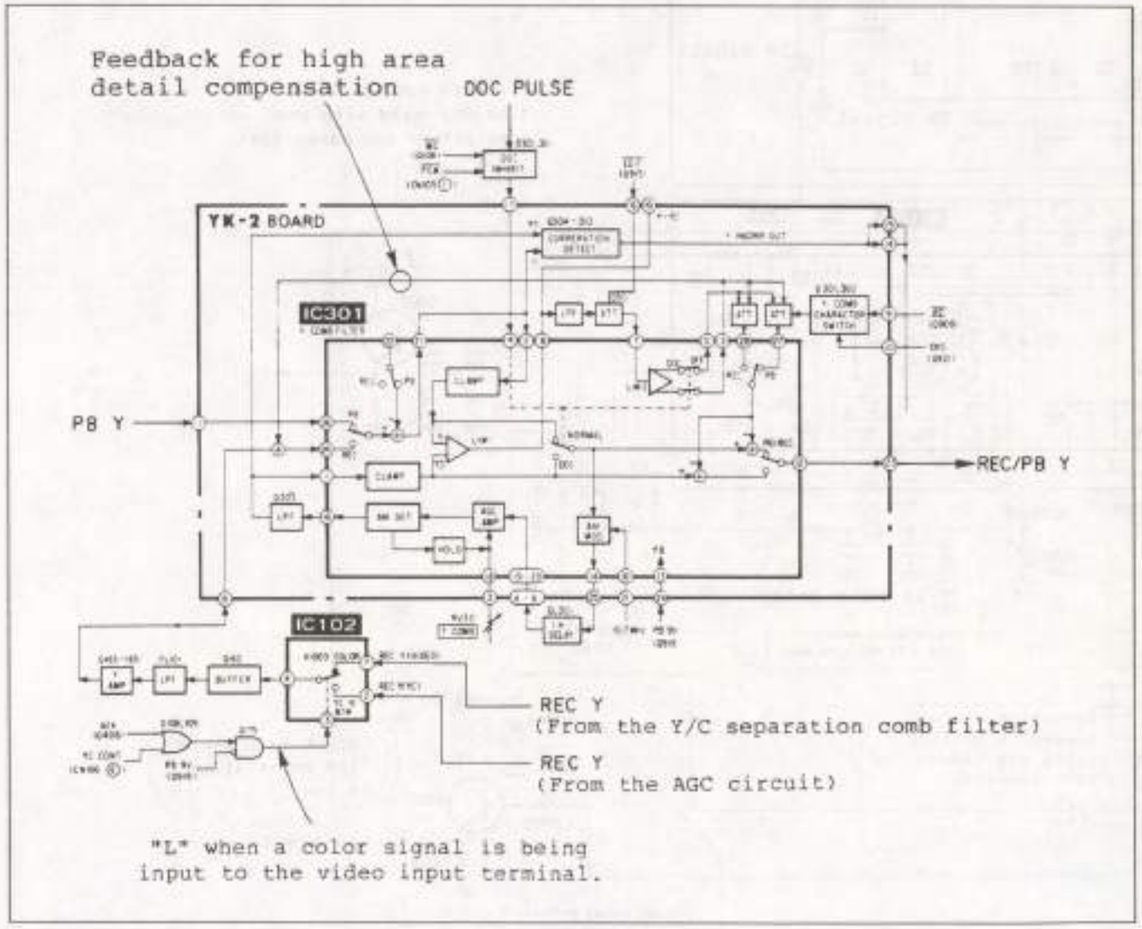


Fig. 1-14

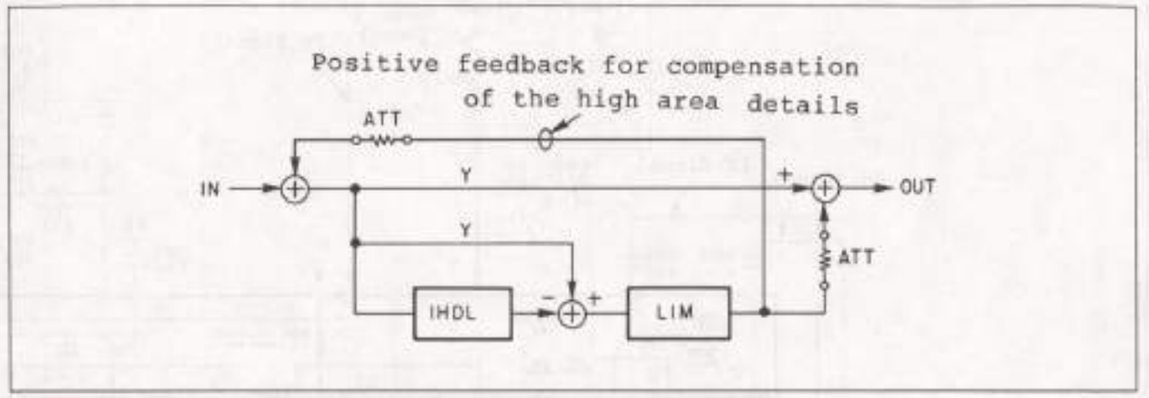


Fig. 1-15 Comb filter principle

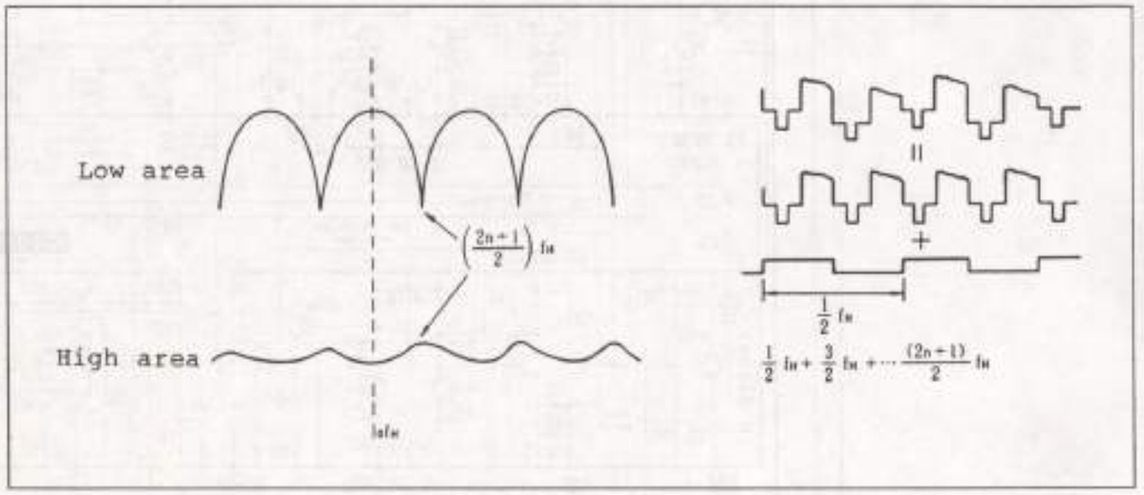


Fig. 1-16 Comb filter response

1-2-5. Pre-emphasis Circuit

The Y signal sync chip clamped in IC101, CX20043 is input to Pin ③ of the PE-4 board and is pre-emphasized. A separate pre-emphasis circuit is used for ED beta and conventional beta and switching is performed by the two power supplies CKG 9V and $\overline{\text{CKG}}$ 9V.

Although ED beta pre-emphasis is a nonlinear pre-emphasis similar to the conventional beta, the amount of emphasis is less and its frequency shifts to the high area. This improves waveform reproducibility in general recording and playback. The decrease in amount of emphasis causes the S/N ratio to drop but this is improved by using a metal tape and increasing deviation.

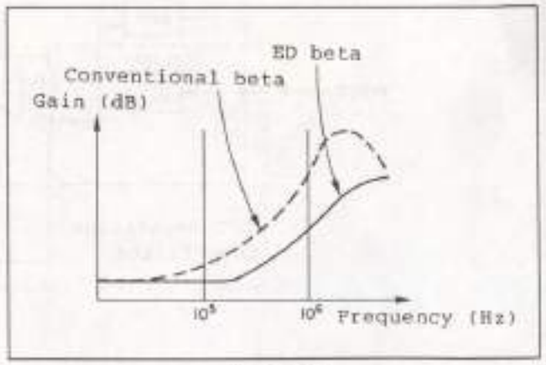


Fig. 1-17

(ED beta pre-emphasis)

The Y signal input to Pin ③ of the PE-4 board passes through Q017 and is input to the base of Q015. The voltage of the VPG signal input of Pin ④ is divided by R048, 049 and 052 at this time and is added to the Y signal for half shift processing. Third order emphasis is applied to the Y signal by the LCR of the Q014 emitter and it is then compressed by the collector load L001, R037, C010, D212 and D213 of Q014. The pre-emphasized signal is converted to a current signal by Q013 and, after passing through R031 and conventional Beta changeover switch D206, it is output to the FM modulator from Pin ⑨.

Q018 and 019 compensates for the temperature characteristics of Q013. Q010 and 011 carries out white clip and its temperature compensation, and Q009, Q008 and D2125 carries out dark clip and its temperature compensation.

Since the amount of emphasis for both white clip and dark clip is small compared to conventional Beta, the amount of clip required is also smalleer compared to the conventional type (White clip = 180%, dark clip = 45%).

(Pre-emphasis of conventional Beta)

The primary emphasis circuit is composed of Q011 and Q002. Q002 operates as a base grounded amplifier. The high area components are reinforced by the CR on the emitter side and is compresed by the pair of diodes on the collector side. The signal from this circuit passes through buffer amp Q003 and enters the base of Q005.

Secondary emphasis is then applied by the CR on the emitter side and third order emphasis applied by the LCR. The emphasis characteristics become the current characteristics of Q005 and enter the current miller circuit configured of transistors Q004 and Q006. In other words, the current with Q005 emphasis characteristics becomes the collector current of Q006. The conventional Beta emphasis characteristic is thus obtained by weighting each of the foregoing emphasis characteristics.

The collector current of Q006 passes through R012 and the ED Beta changeover switch D206 and is output from Pin ⑨ and drives the FM modulator. R004, 005 and 007 add VPG signals to the Y signal for half H shift. The half H shift provides a 1/2 fH frequency difference to the Y-FM signal frequency of the adjacent track and thus reduces crosstalk during playback.

D210 and 211 carry out white clip and Q007 and D202 carry out dark clip. D203 is a carrier shift switch that raises the carrier frequency when Beta HiFi and SUPER BETA.

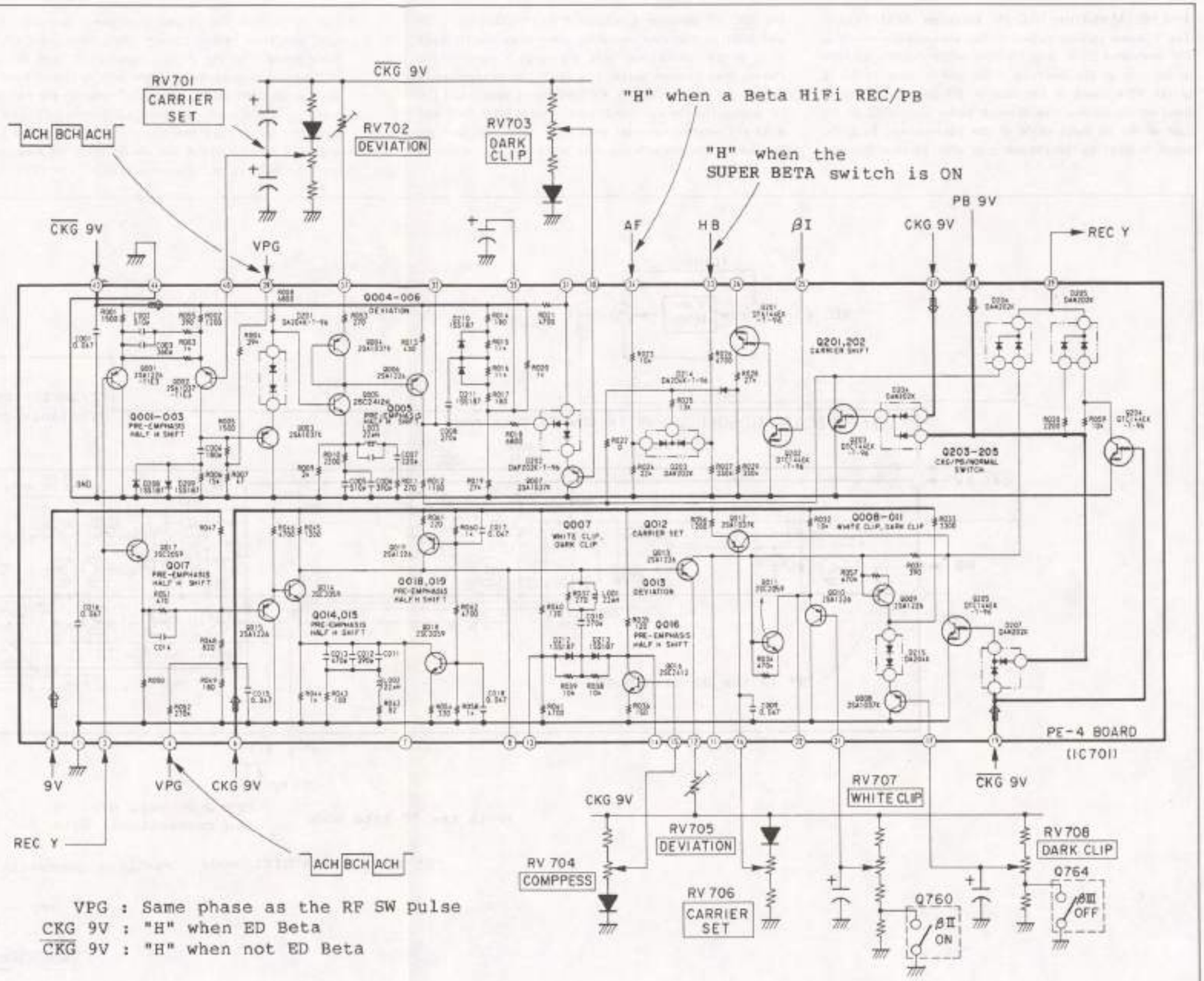


Fig. 1-18

1-2-6. Modulator, REC RF Equalizer, AFM Trap

The Y signal current output of the pre-emphasis circuit is FM modulated (Sync chip 6.8 MHz, white (100%) 9.3 MHz in the case of ED Beta) by IC101 and is input to Pin ⑫ of the YF-2 board. In the case of ED Beta, the signal is input to the chroma trap through buffer amp Q020. In the case of the Hi Band mode of the conventional Beta, the signal is input to the chroma trap after passing through the REC RF equalizer composed of Q018, 019, L008, C028 and R051. In the case of modes other than the Hi Band mode of the conventional Beta, the signal is input to the chroma trap through buffer amp Q017. This changeover is carried out by the CKG 9V, $\overline{CKG}$ 9V power supply and the HB signal. The chroma trap is configured of L009, C033 and R053 and serves to prevent cross color during playback by attenuating the 688 kHz signal to which the chroma signal is added.

The signal from the chroma trap circuit is amplified by Q021 and, after passing through Q022, R070 and C037 and being mixed with the chroma signal input from the peak ACC narrier trap circuit through Q023, is output from Pin ⑯. Since the Q022 base becomes "H" when in the Beta HiFi mode of the conventional Beta, Q022 goes OFF and the signal passes through the trap circuit composed of L602 and C610 between Pin ⑱ and Pin ⑲ where the frequencies near the AFM carrier frequency (1.38 – 1.83 MHz) are attenuated to minimize effects on the audio signal. The AFM carrier frequency differ for Ach and Bch so the attenuating frequency of the trap is changed by switching Q604 with the VPG signal.

Q025 and 212 go ON in the ED Beta mode and increases the recording current of the Y signal and chroma signal. Q029 and 211 go ON during overwrite and increases the Y signal and chroma signal currents.

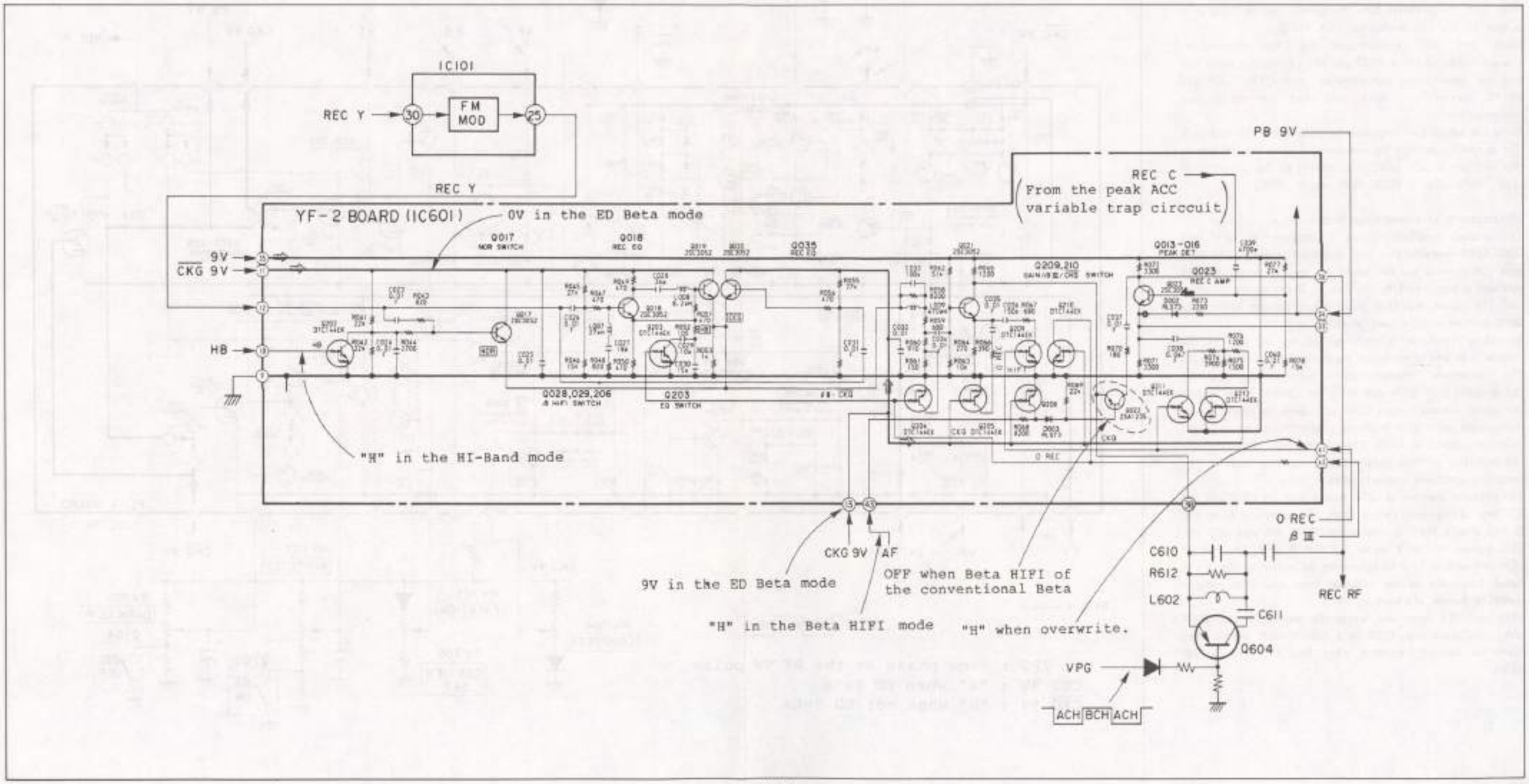


Fig. 1-19

1-2-7. REC Amp

Since metal tapes require twice the recording current of conventional tapes, the newly developed CXA-1091M is used for the REC/PB amp (IC001 of the RP board).

The REC RF signal is amplified by Q010 and is input to Pin ⑯ of IC001 after its recording current is set by RV001. The signal is split in the IC with the signal for the Bch output from Pin ⑫. This signal is then mixed in Q007 with the AFM signal for the Bch (REC AF B), and is reinput from Pin ⑪. The mixed signal is V-I converted and output from Pin ⑬ after passing through the REC amp. The following Q001 is a transistor for dynamic range expansion. That is, IC001 is only capable of outputting a maximum of 5 Vp-p since it is a 5 V IC so Q001 is used so it can drive transformer T001 with a 9 V power supply. The signal passing through Q001 and T001 is supplied to the video head through the rotary transformer. The foregoing process is the same for the A CH.

D001 goes OFF during playback and eliminates loss of the playback signal.

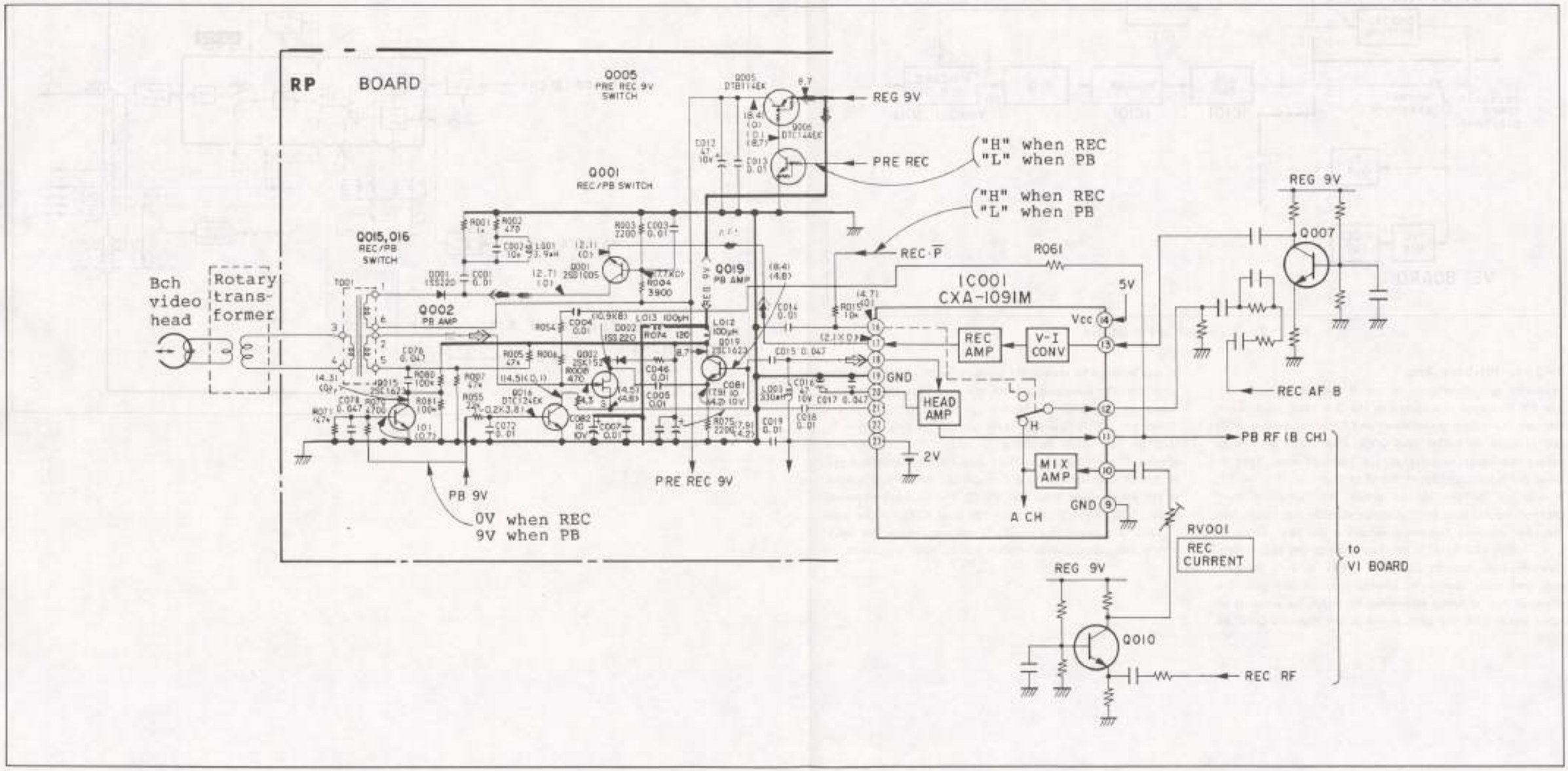


Fig. 1-20

1-3. PLAYBACK SYSTEM OF THE Y SIGNAL

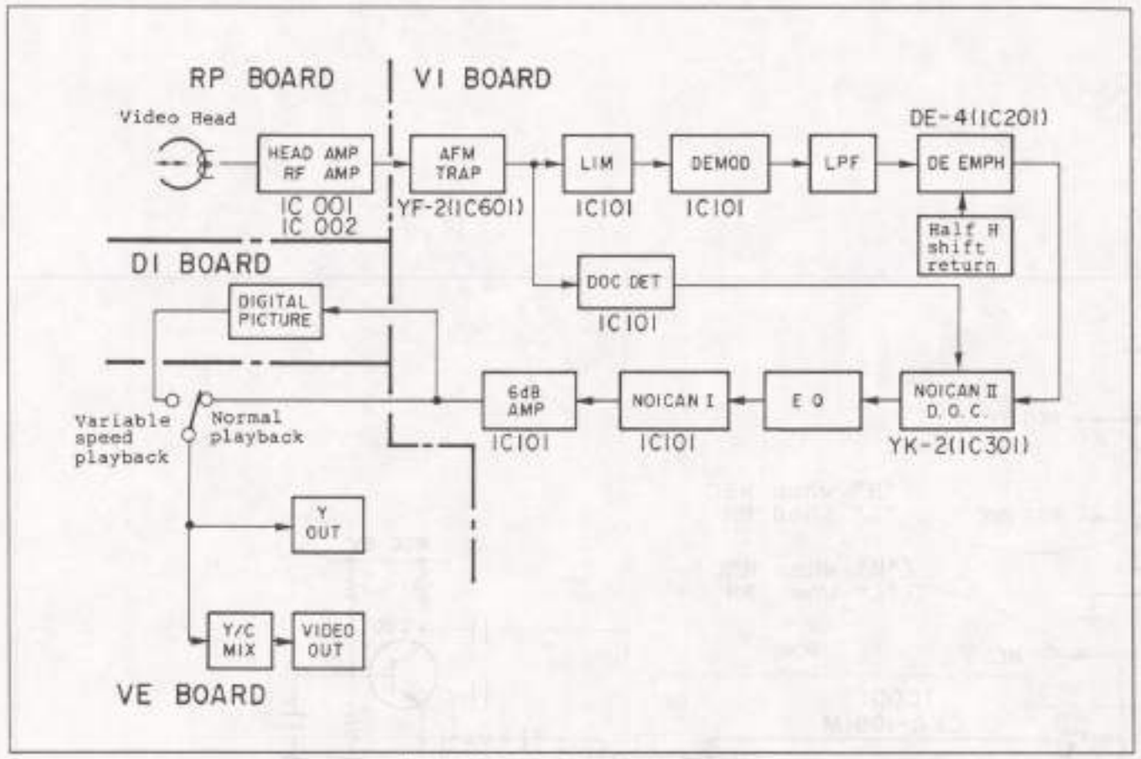


Fig. 1-21 Y playback circuit diagram

1-3-1. Playback Amp

Following is a description of the B channel.

The PB RF signal reproduced in the Bch video head passes through the rotary transformer and I/O transformer T001 and is input to buffer amp Q002. This buffer amp is to reduce the input capacity of the playback amp. That is, since the input capacity of Pin ⑬ of IC001 is 50 – 60 PF, it will not be possible to obtain the frequency band required for ED Beta by connecting directly due to the fact that the resonant frequency including the head drops to 6 – 7 MHz. FET Q002 is therfore used as the buffer amp. However, since capacity Cgd (2 – 3 PF) between the FET gate and drain cannot be ignored even in this case, the effect of Cgd is being eliminated by supplying a signal of equal phase with the gate signal to the drain of Q002 by Q019.

It was possible to reduce the input capacity of the playback amp with the foregoing process and thus raise the resonant frequency including the head to about 13 MHz.

Althoughy Q015, 016 and D002 are ON during playback, they go OFF when recording to protect the PB amp and eliminate recording current loss. The PB RF signal is input to Pin ⑯ and, after passing through the PB amp, is output to the PB equalizer amp from Pin ⑪. The feedback elements (R061, C004, R054, R006) from Pin ⑪ of IC001 to the gate of Q002 attenuates the feedback and suppresses the peak of the frequency characteristics due to head resonance.

1-3-2. Playback Equalizer Amp

As in the past, the CX-893A is used for the playback equalizer amp. Gain switches Q021 and 022 are ON in the ED Beta to equalize the playback level with the conventional Beta. The equalizer elements of Pins ⑧ and ⑨ of IC002 are for ED Beta use. A separate equalizer circuit composed of Q001 is provided outside the IC for the conventional Beta.

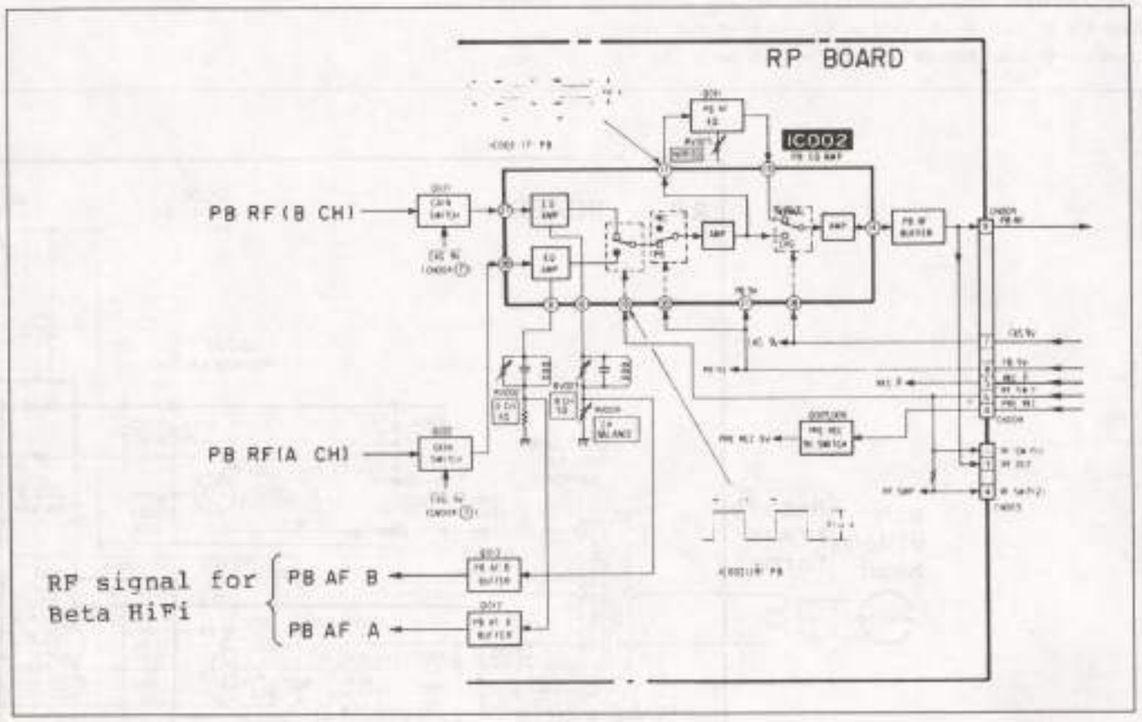


Fig. 1-22

1-3-3. AFM Trap

The PB RF signal is input to Pin ③ of the YF-2 board and, after being amplified in Q024 and 025 and passing through the AFM trap, is split into signals for the Y signal system and the chroma signal syste. The AFM trap is composed of FL001 and FL002 with QG26 provided between the two traps for impedance matching. When playing back tapes which are not recorded with Beta HiFi of the conventional Beta, the AF signal becomes "L", Q028 goes OFF, Q029 goes ON and the playback signal does not pass through the AFM trap.

1-3-4. Soft Limiter

The unwanted bands above 15 MHz of the PB RF signal are removed in the low pass filter composed of L011, C049 and C051. The PB RF signal then passes through Q030 and the chroma trap (688 kHz) formed of L012 and C052 and is input to the soft limiter configured of Q032, D104 and 105 after passing through Q031. The soft limiter reinforces the high area of the frequency when the RF signal level is low and thus prevents the inversion phenomenon. An HPF composed of C604 and a resistor is connected to Pins ⑱ and ⑲ of the YF-2 board. This HPF changes its characteristics in accordance with each mode and also heightens the preventive effects sof the inversion phenomenon. This signal is reinput to the YF-2 board and is output to the FM demodulator after passing through the LPF configured of Q033, 034, L014, C060 and 061.

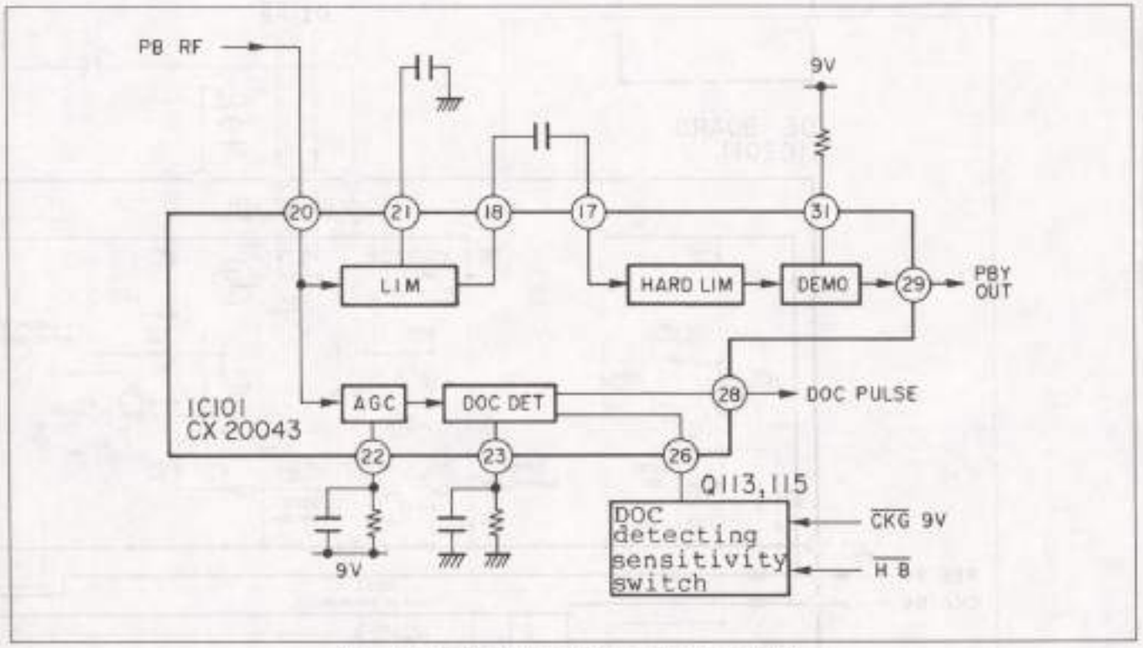


Fig. 1-24 Demodulator/Dropout ditection circuit

1-3-5. FM Demodulation/Dropout Detection Circuit

The Y-RF signal input from Pin ㉝ of IC101 is sent to the hard limiter and DOC detector. The signal to the hard limiter enters the FM demodulator and is output from Pin ㉙. The demodulated signal passes through the LPF and is sent to the de-emphasis circuit. In the DOC detector, AGC is applied to the RF signal and envelope is detected after setting to a fixed level. The DOC output is sent to the YK-2 board (IC301) where dropout compensation is carried out. The operating circuit is shown in Fig. 1-24.

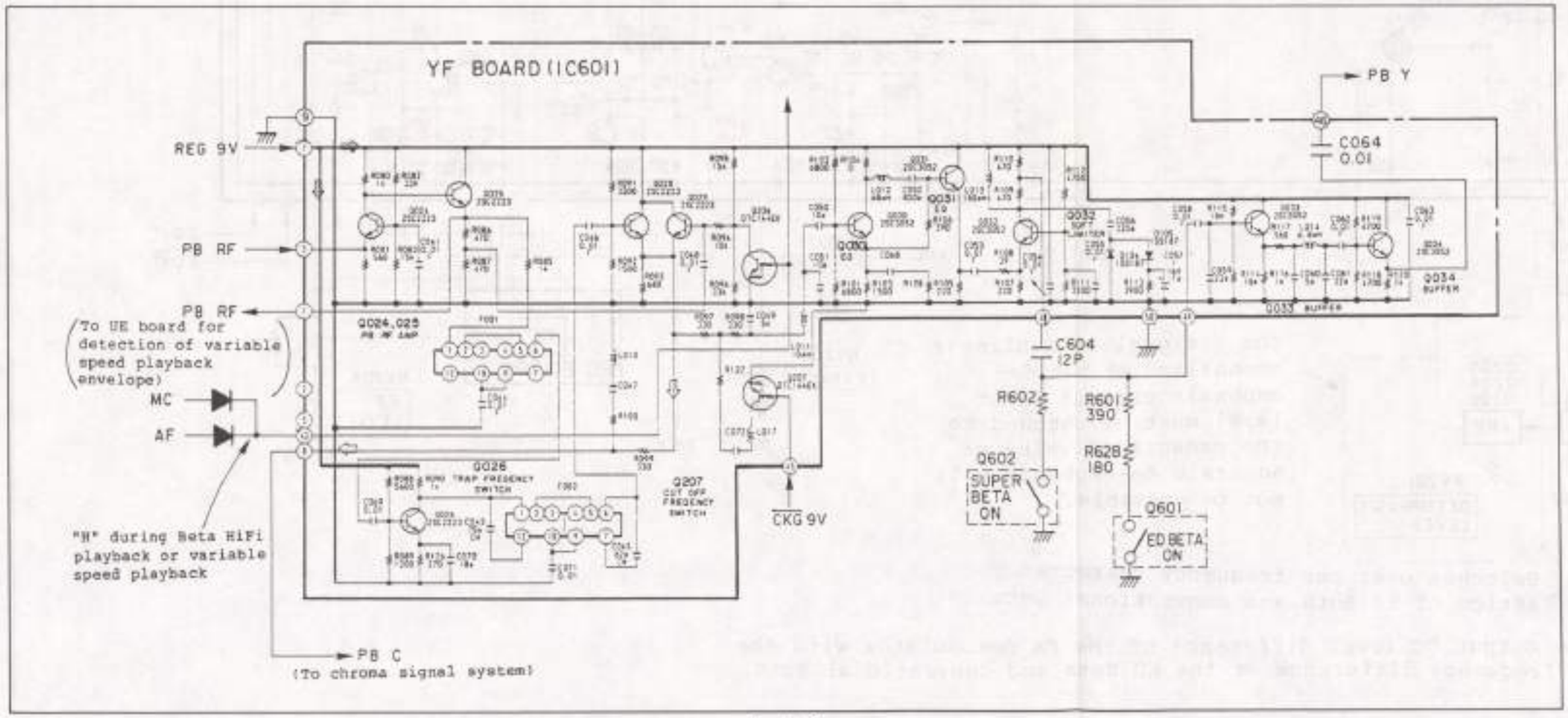


Fig. 1-23

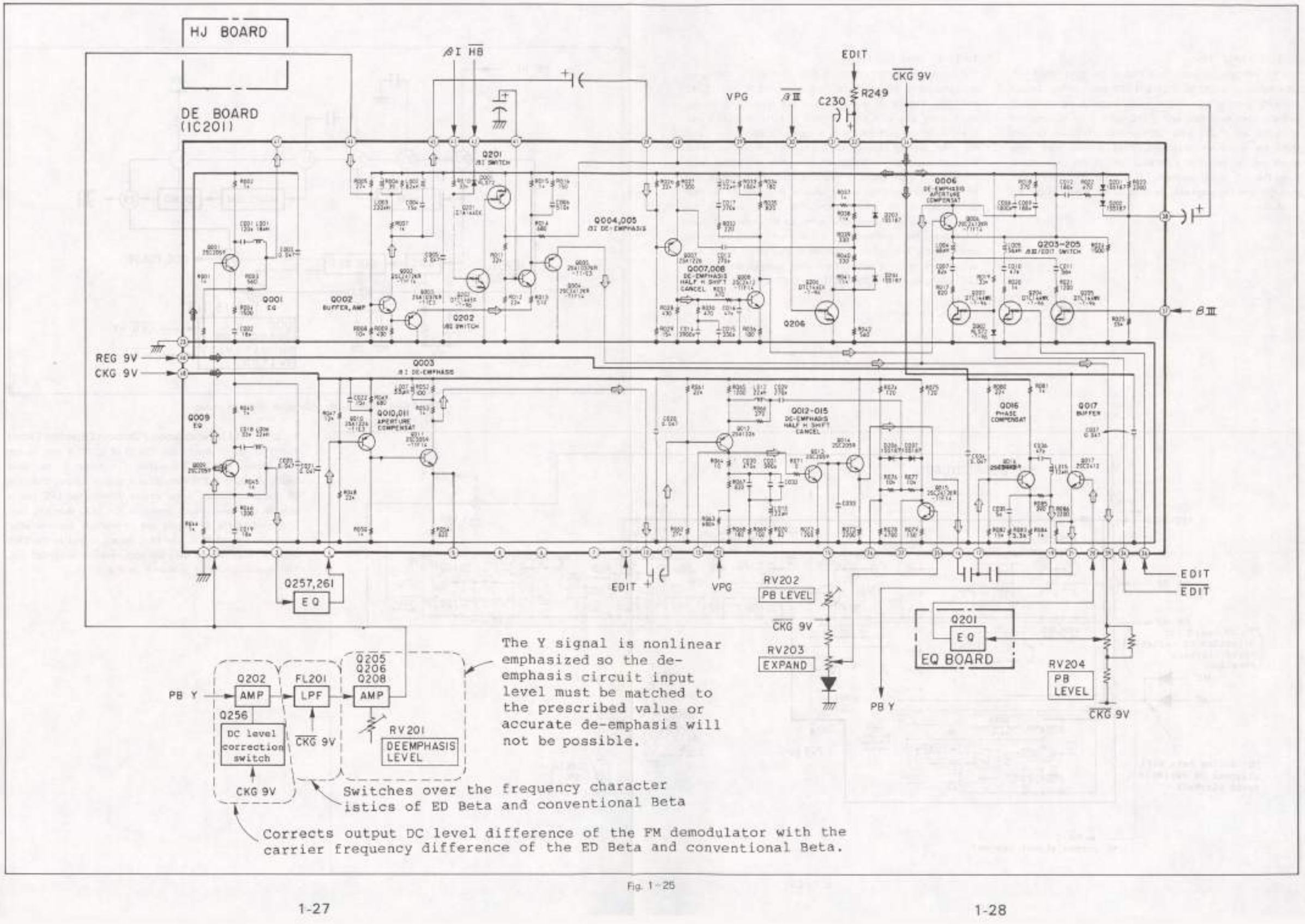

HJ BOARD
DE BOARD
(IC201)
ØI HB
EDIT
CKG 9V
VPG
ØII
C230
R249
Q201
ØI SWITCH
Q004,005
ØI DE-EMPHASIS
Q006
DE-EMPHASIS
APERTURE
COMPENSAT
Q203-205
ØII/EDIT SWITCH
Q007,008
DE-EMPHASIS
HALF H SHIFT
CANCEL
Q206
Q001
EQ
Q002
BUFFER AMP
Q202
ØI SWITCH
ØIII
REG 9V
CKG 9V
Q003
ØI DE-EMPHASIS
Q009
EQ
Q010,011
APERTURE
COMPENSAT
Q012-015
DE-EMPHASIS
HALF H SHIFT
CANCEL
Q016
PHASE
COMPENSAT
Q017
BUFFER
Q257,261
EQ
EDIT
VPG
RV202
PB LEVEL
CKG 9V
RV203
EXPAND
PB Y
Q201
EQ
EQ BOARD
RV204
PB
LEVEL
CKG 9V
EDIT
EDIT
PB Y
Q202
AMP
Q256
DC level
correction
switch
CKG 9V
FL201
LPF
CKG 9V
Q205
Q206
Q208
AMP
RV201
DEEMPHASIS
LEVEL
The Y signal is nonlinear emphasized so the de-emphasis circuit input level must be matched to the prescribed value or accurate de-emphasis will not be possible.
Switches over the frequency characteristics of ED Beta and conventional Beta
Corrects output DC level difference of the FM demodulator with the carrier frequency difference of the ED Beta and conventional Beta.

Fig. 1-25

1-3-6. De-emphasis Circuit

Similar to the pre-emphasis circuit, the de-emphasis circuit is divided into the circuit for ED Beta and that for conventional Beta.

The PB Y signal output from the FM demodulator through an LPF to remove the FM carrier and through a de-emphasis input level adjusting circuit, and is input to Pin ㉒ of the DE-4 board (IC201). The frequency band of the LPF is changed over for ED Beta and conventional Beta. The de-emphasized Y signal (Pin ㉓ output in ED Beta and Pin ㉑ output in conventional Beta) is reinput to Pin ⑰ and is output from Pin ⑱ to the sharpness control circuit after passing through the equalizer circuit. Switching between ED Beta and conventional Beta is conducted by the CKG 9 V and $\overline{\text{CKG}}$ 9 V power supplies.

(ED Beta de-emphasis circuit)

Phase distortion of the Y signal occurring in the LPF (FL201) is corrected by Q009 in the DE board and the equalizer circuit (Q250, 251) connected to Pins ㉛ and ㊶. Frequency characteristics are then corrected by Q010 and 011 and the signal is input to the base of Q012. The signal is expanded by L012, R066, C029, D206 and D207 of the Q012 emitter and de-emphasized by the LCR of the collector. These characteristics are exactly opposite to the compressed and pre-emphasis characterisitcs during playback and improve the waveform reproducibility. Half shift return processing is carried out on the collector of Q012 with the addition of the VPG signal by means of R036 and R068. The signal is then input to the base of Q013 where it is adjusted to playback level by RV202 of the collector. It is then output to Pin ⑯ through Q014.

(Conventional Beta de-emphasis circuit)

Y signal is input to Q002.

In the β II, β III and β I s modes, the signal is expanded by the Q007 emitter after its high area is slightly emphasized by L003. This is a reverse conversion of white clip during recording with expand II. Nonlinear de-emphasis is being carried out using the diode characteristics of D203 and D204. In the β III mode, Q206 goes OFF and edge noise is made inconspicuous by R042. When in the EDIT mode, inverse bias is aplied to the diode by R249 to obtain optimum waveform. The signal with Expand II applied passes through de-emphasis II composed of R028, R030, C014 and C015 on the collector of Q007. The LPF composed of R031 and C016 is inserted for the purpose of removing unwanted waveform whisker components generated in Expand II.

The signal from De-emphasis II passes through De-emphasis III composed of L014, C017 and R032 on the collector of Q008 and is input to Q006 after passing through the half shift return composed of R033 and R034.

Although high emphasis and Expand I processing is being conducted, L004, C007 and R017 operate in the β II and β I s modes since Q203 goes ON, and L004, C007, R017, C011 and R021 operate in the β III mode since Q203 and Q205 go ON.

In the EDIT mode, L005, C010 and R020 operate since Q203 goes OFF and Q204 goes ON. Optimum picture quality is therefore obtained by changing over according to the mode. Expand I corresponds to Compress I when recording with nonlinear de-emphasis using the diode characteristics of D201 and D202.

The signal passing through Expand I passes through De-emphasis I composed of R018, C008 and C009 on the collector of Q006 and, after its playback output is adjusted by RV204, it passes through the equalizer of Q201 of the EQ board and is output to Pin ㉔ after passing through Q017. When in the β I mode, current is supplied to R024 through R014 since Q201 and Q202 goe ON, and Q006 is cut off. At the same time, the signal is input to the base grounded amp Q004 from the emitter of Q003 without passing through the nonlinear de-emphasis circuit since Q004 goes ON and is output to the emitter of Q005 after passing through the linear de-emphasis circuit composed of R015, R016 and C006. De-emphasis will also be nonlinear in the β I mode if the SUPER BETA switch is ON (β I s mode) because Q004 goes OFF.

1-3-7. Sharpness Control Circuit

The PB Y signal passes through buffer amp Q250 and is grounded-base amplified by Q254 after passing through R265. Apart from this, the profile component signal is extracted from the PB Y signal by L251 and C261 and is grounded-emitter amplified by Q254. Both signals will therefore be added on the collector of Q254 and a profile corrected signal will be output.

The amount of profile correction will be determined by the impedance of the emitter of Q254. Sharpness control is therefore carried out by adjusting the bias current of the variable impedance elements D253 and D254 with RV301.

The inpedance of D253 and D254 will be infinitely large during the EDIT mode since Q252 will go OFF. However, Q251 goes ON and R265 determines the amount of profile correction.

1-3-8. Dropout Compensating Circuit

The Y signal from the sharpness control circuit is applied to Pin ㉘ of IC301 and, after passing through the clamping circuit and having the Y_D signal deducted, it is output from Pin ㉜. On one hand, the Y_D signal AM modulates the Y signal at 10.7 MHz and appears at Pin ㊴ after passing through 1H DL and the AGC and detector circuits. This Y_D signal passes through the clamp circuit where the Y-Y_D signal is deducted and this difference is output from Pin ㉑ as a correlation signal. The dropout compensation circuit is shown in Fig. 1-27.

Noise components can also be removed similar to the noise cancelling circuit by subracting the Y-Y_D signal from the Y signal and also remove crosstalk from the 0.5 H shifted adjacent track. The output signal on Pin ㉜ is switched over to a Y_D signal by the DOC PULSE input to Pin ㉑ and at the same time, subraction of the Y-Y_D signal from the Y signal stops and dropout compensation is carried out. To enable the video signal to compensate for the dropout portion, the circuit is arranged so white noise and black noise do not appear on the playback screen. A block diagram of the comb filter is shown in Fig.28. Q304 – 310 detects the Y-Y_D signal level and outputs this to the CF-3 board (IC801). Operation of the chroma comb filter is suppressed when the line correlation of the Y signal is low thus preventing "color runs" of the chroma signal.

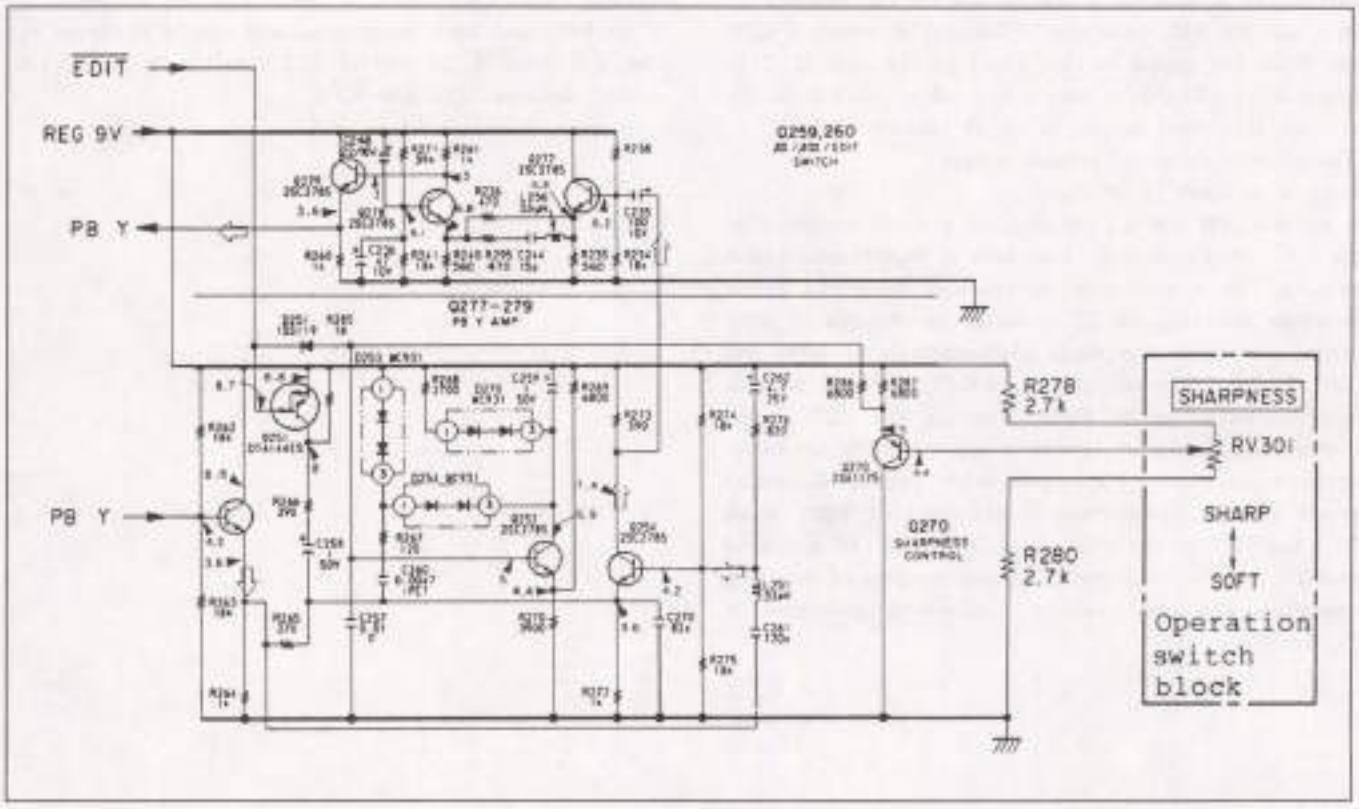


Fig. 1-26

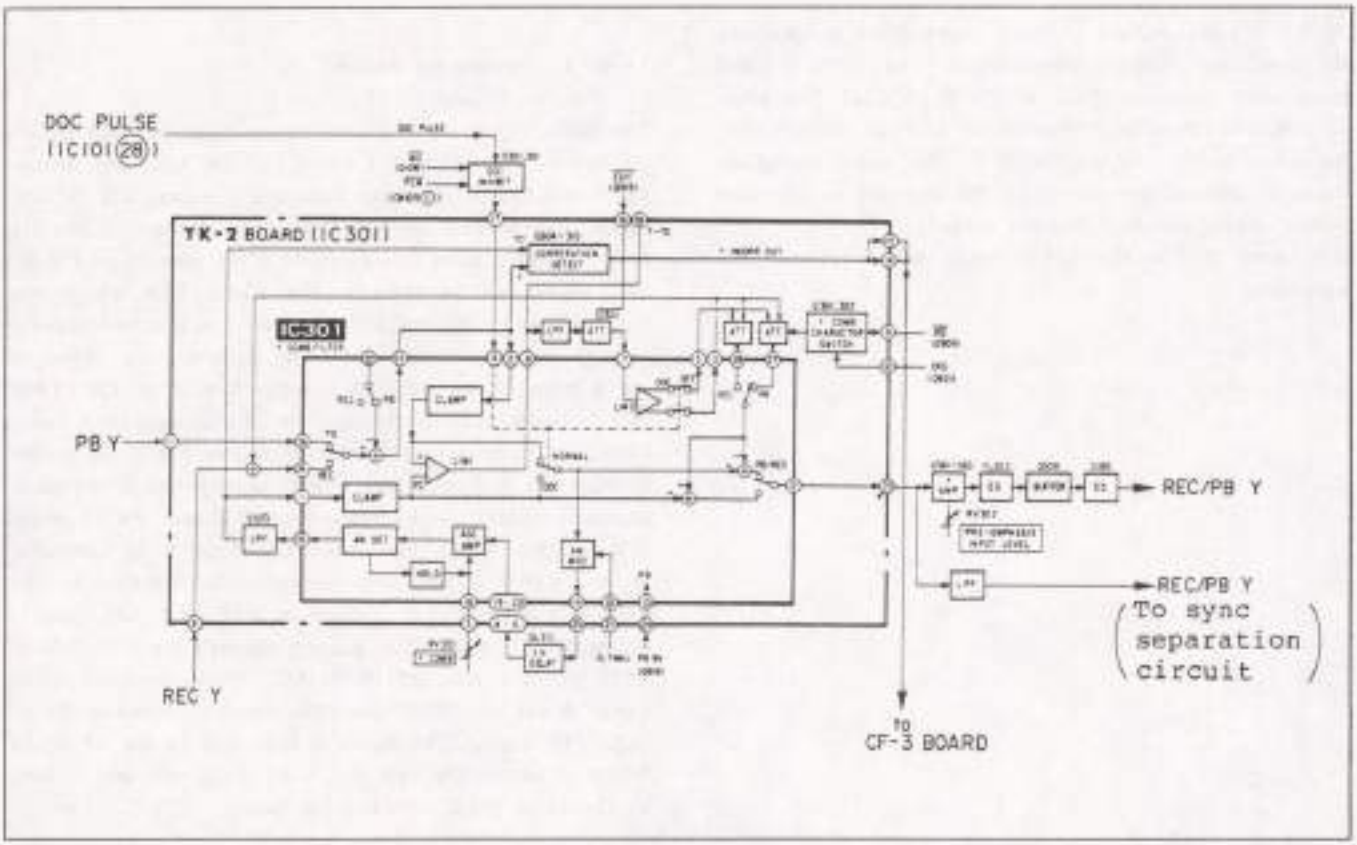


Fig. 1-27 Dropout compensation circuit

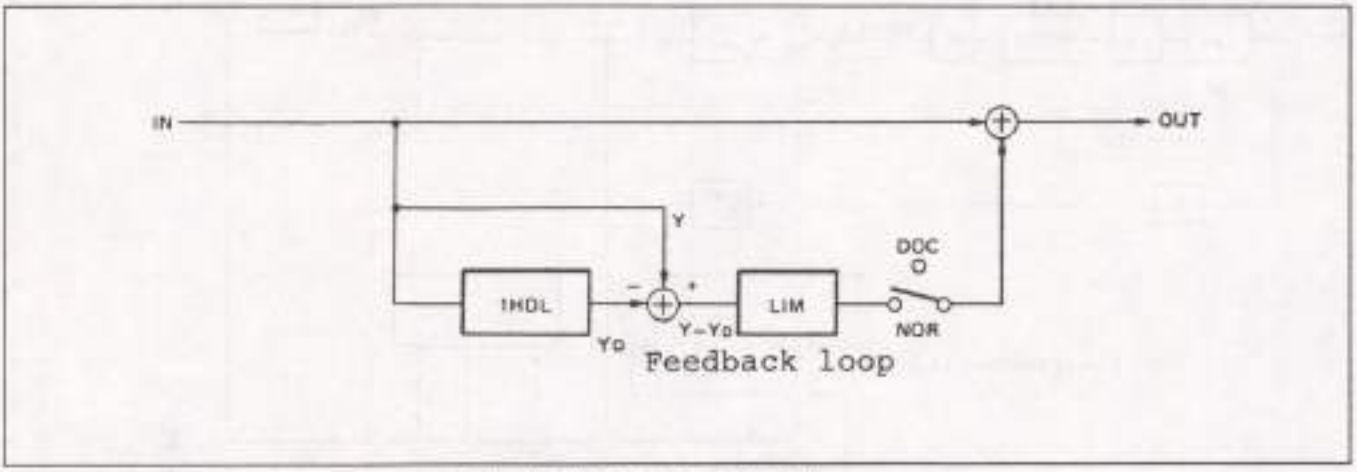


Fig. 1-28 Comb filter block diagram

1-3-9. Noise Cancelling Circuit

The PB Y signal output of the Y comb filter divides into two. One pases through the equalizer circuit and is input to the noise cancelling circuit of Pin ㊴ of IC101. The other is input to the sync separation circuit through the CR LPF. The amount of noise cancelled in the noise cancelling circuit is changed over by Q103, 105 and 107 so optimum picture can be obtained in each mode.

Q110 goes ON in the EDIT mode and inhibits noise cancellation.

1-4. CHROMA SYSTEM CIRCUIT

1-4-1. Recording Mode

See Figs. 1-30 and 1-32.

The video signal input to the image input terminal enters the comb filter of the VI board via the AGC amp of the VE board and is separated into the Y signal and chroma signal. The chroma signal obtained by subracting the 1H previous signal from this signal in IC101 appears on Pin ㊱. This signal passes through the FL402 BPF where the reduced components of the Y signal are removed, leaving only the chroma components. The chroma signal input to the S image input terminal is input directly to the FL402 BPF without passing through the Y/C separation comb filter. The chroma signal enters Pin ㊶ of IC401 and passes through the ACC amp where burst is amplified in the burst emphasis circuit to +1.5 dB when β II and +6 dB when β III and the signal then enters Converter II. In Converter II, the signal is low ares converted to 688 kHz by the 4.27 MHz idler signal created in APC and AFC and is output from Pin ㊳. After passing through the LPF,(3.58 + 4.27) MHz trap and the PEAK ACC circuit, the level of the signal is set by RV601 and the signal is mixed with the REC Y-RF signal. The signal is then sent to the RP board where it passes through the IC001 REC amp and is sent to the video head recording on tape.

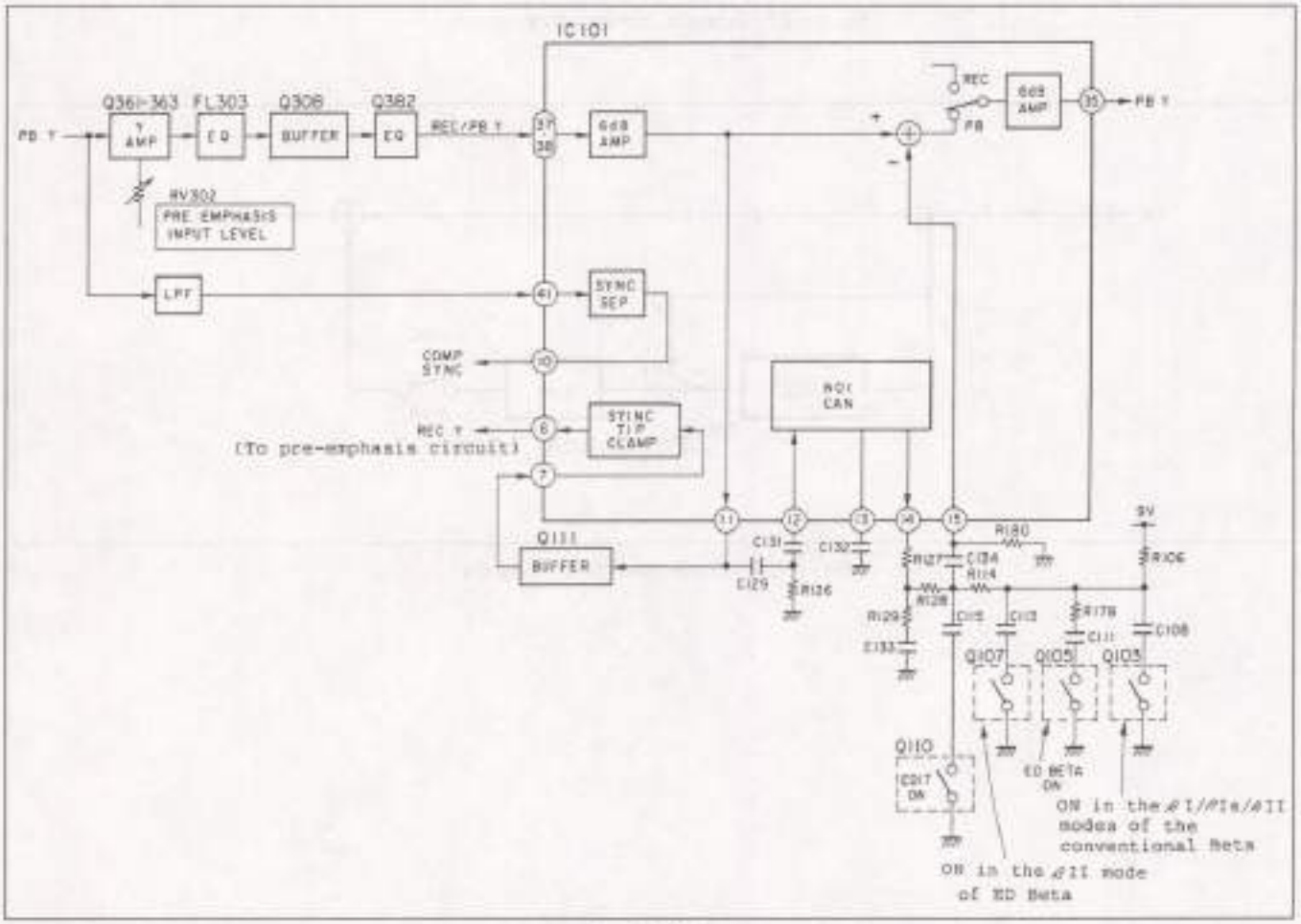


Fig. 1-29

1-4-2. Playback Color Mode

The playback RF video signal passes through the PB amp of IC001 and 002 of the RP board and enters the VI board. It then passes through the AFM trap circuit for playback and enters Pin ⑦ of IC401 after passing through T401 and the LPF. The low pass chroma signal from Pin ⑦ passes through the ACC amp and enters the burst emphasis circuit where burst is attenuated and the signal then enters Converter Ⅱ. The amount of burst emphasis is matched with that of Q402 of the CH board in a later stage and is −0.5 to 1.0 dB in the βⅡ mode and −3.5 to −4.0 dB in the βⅢ mode. The 3.58 MHz chroma playback signal is created by the 4.27 MHz idler signal created in Converter Ⅱ by APC and VXO for frequency conversion and is output from Pin ㉚. The unwanted band components are removed from this 3.58 MHz chroma signal by the BPF (FL401). The signal then enters Pin ⑪ of IC101 and is output from Pin ⑭ after passing through the comb type circuit where the crosstalk components are cancelled. The burst in the chroma signal from IC101 is again attenuated by Q402 of the CH board and the signal is then input to Pin ㉑ of IC401. The signal passes through the chroma inverter controlled by the burst ID and is output to Pin ㉓ as playback chroma signals after passing through ACK. It is then input to the VE board where it is mixed with the Y singal.

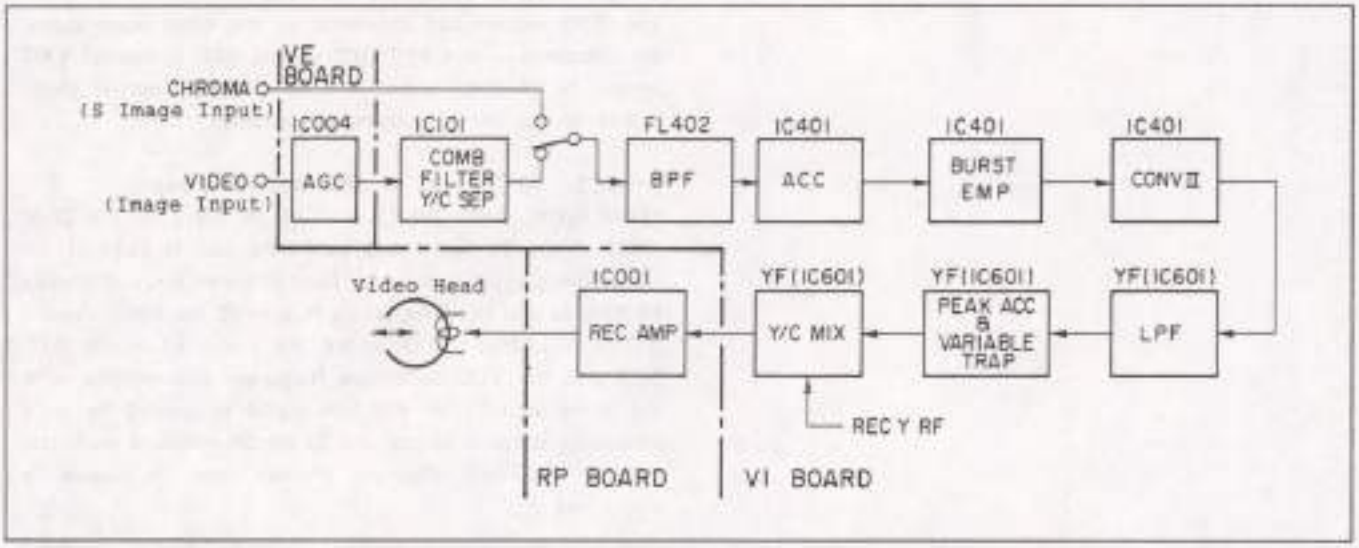


Fig. 1-30 Chroma recording system block diagram

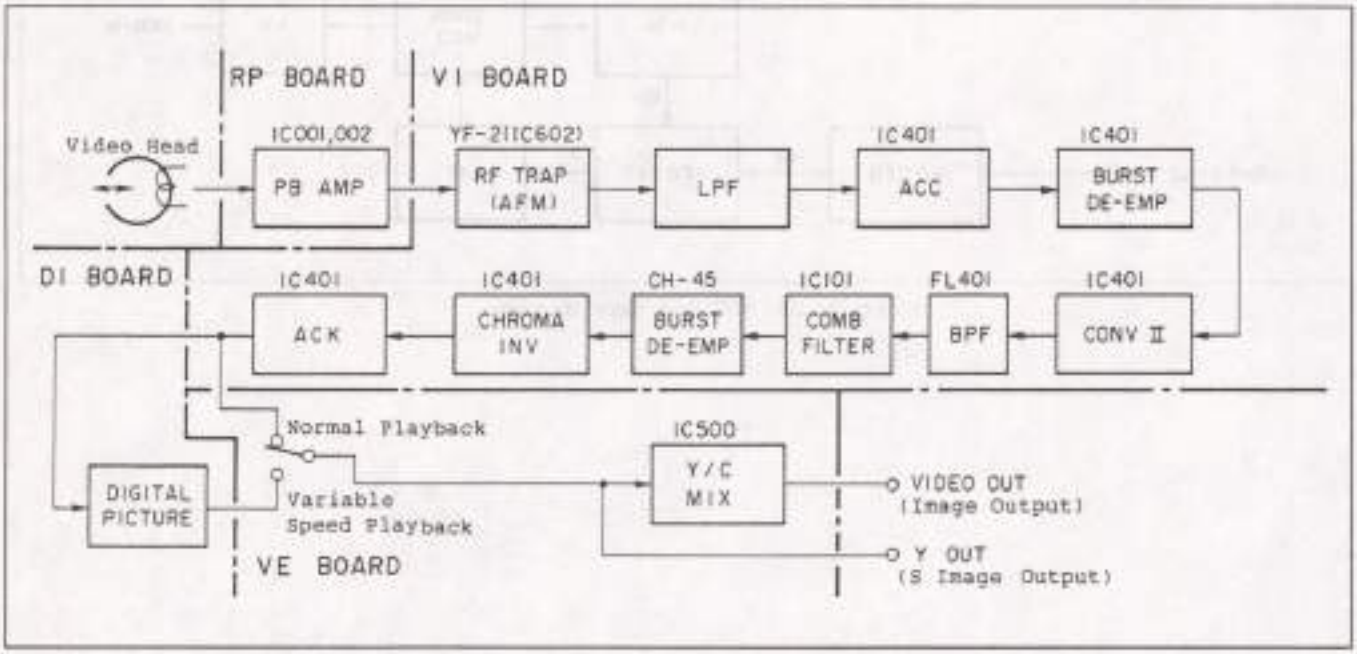


Fig. 1-31 Chroma playback system block diagram

1-4-3. ACC Circuit

The ACC amp output enters the ACC DET during REC, and the chroma signal converted to 3.58 MHz from the chroma INV enters the ACC DET during PB and controls the ACC amp so the burst level in the ACC of Pin ⑪ of IC401 of the VI-40 board is 700 mVp-p.

Since the burst level of CH HOLD is fixed for each field during REC, only one side (Pin ⑧ of Bch) is used.

Q405 and 416 are switched by the MC signal and the time constant of Pins ⑥ and ⑧ of IC401 shortened for high speed ACC to reduce chroma flicker during variable speed palyback.

1-4-4. APC Circuit when REC

The VXO output and the burst of the video input signal are compared in the APC DET during REC to control VXO so will be of equal phase. A 3.58 MHz VXO output phase locked to the burst is therefore obtained.

1-4-5. AFC Loop of the Record Mode

COMP SYNC from Pin ⑲ of IC101 is input to Pin ㉒ of IC401 of the VI board and masks the half H pulse of the signal being synchronized by the HD generator, and creates fH. This fH and the 5 fH, which is a 1/70 frequency divided 350 fH (5.5 MHz) VCO output are compared in the AFC DET and the VOC oscillation frequency is controlled with the error signal. The 688 kHz signal is created by 1/8 frequency division of the 350 fH signal stabilized with this control. A block diagram of this loop is shown in Fig. 1-33.

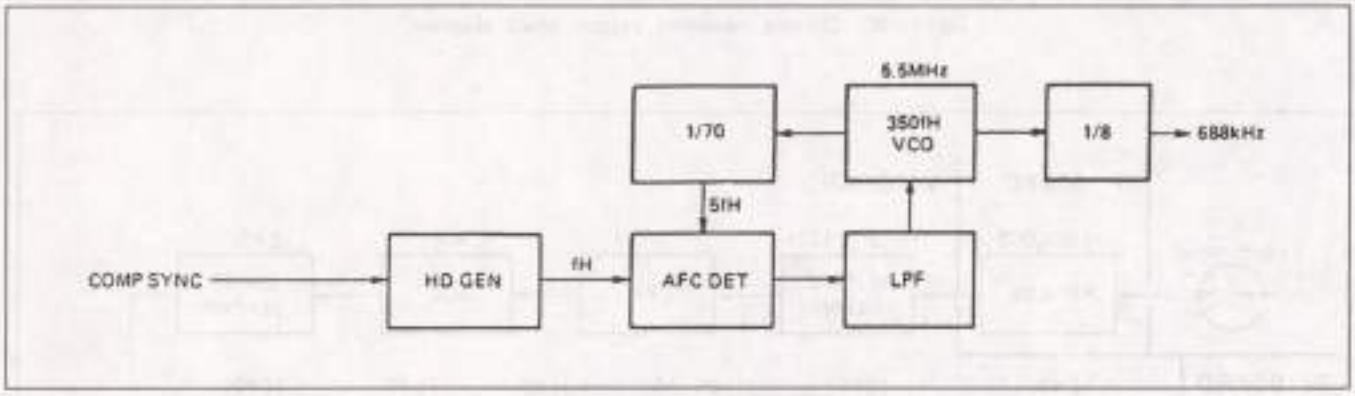


Fig. 1-33 AFC loop block diagram

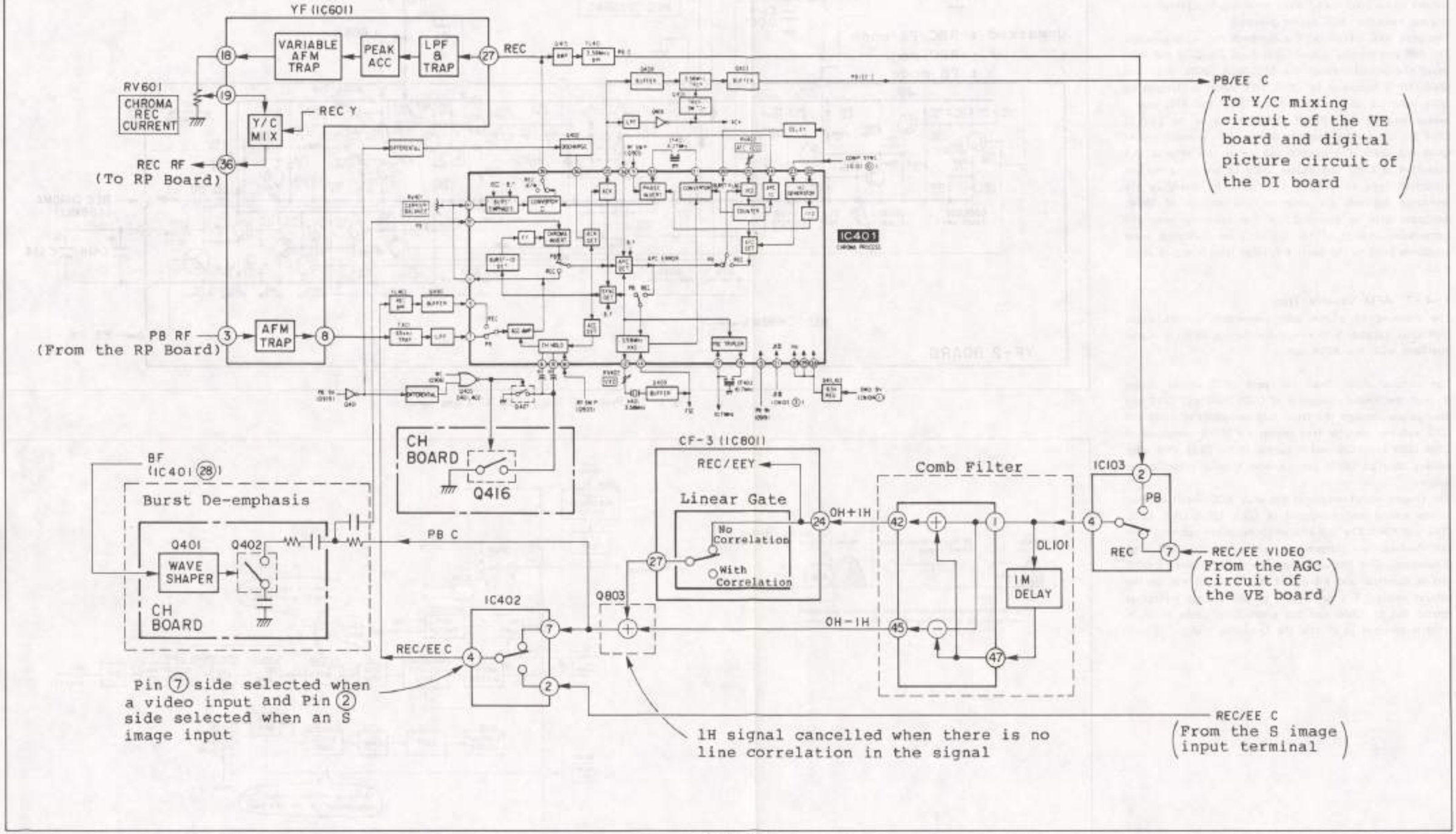

YF (IC601)
VARIABLE AFM TRAP
PEAK ACC
LPF & TRAP
REC
18
27
RV601
CHROMA REC CURRENT
19
Y/C MIX
REC Y
REC RF
(To RP Board)
36
PB RF
(From the RP Board)
3
AFM TRAP
8
PB/EE C
To Y/C mixing circuit of the VE board and digital picture circuit of the DI board
IC401
CHROMA PROCESS
CH BOARD
Q416
CF-3 (IC801)
REC/EEY
Linear Gate
No Correlation
With Correlation
24
27
0H+1H
Comb Filter
42
1
45
47
DL101
1M DELAY
IC103
2
PB
4
REC
7
REC/EE VIDEO
From the AGC circuit of the VE board
BF
(IC401 (28))
Burst De-emphasis
Q401
Q402
WAVE SHAPER
CH BOARD
PB C
IC402
7
4
2
Q803
0H-1H
REC/EE C
Pin (7) side selected when a video input and Pin (2) side selected when an S image input
1H signal cancelled when there is no line correlation in the signal
REC/EE C
From the S image input terminal

Fig. 1-32

1-4-6. Peak ACC Circuit

Peak ACC is a circuit to improve chroma S/N when recording by increasing the recording current where the color is light on the screen (chroma level is low). The chroma signal level raised when recording is returned to its original value by ACC during playback.

The peak ACC circuit is of a feedback loop configuration. The 688 kHz chroma signal input from Pin ㉑ of the YF-2 board and passed through the LPF, VCA (Q009, 010) and Q006, 007 is branched by Q013. This signal is clamped by Q014, detected and integrated by Q015 and 016, and is passed through the LPF of C614 for use as the LPF of C614 for use as the control voltage of VCA composed of Q008 and Q009. The control voltage at this time is V-A converted in Q008 and causes Q008 to become a current attraction type to control VCA gain by changing the resistance between the collector and emitter of Q008. Adequate gain is provided for the feedback loop and compression change of the circuit from maximum color amplitude level to the burst P-P value level is set at about 6 dB.

1-4-7. AFM Variable Trap

The sideband of a low area conversion chroma signal (688 kHz) expands with rise in the chroma signal level and interferes with the AFM signal.

The chroma signal from the peak ACC circuit passes through the limiter composed of D101, D102 and C010 and then passes through the fixed trap composed of L004 and C012 and the variable trap (about 1.4 MHz) composed of D103, L003 and C009, and is output to Pin ⑱ of YF-2 after passing through Q012. The variable trap is controlled as follows.

The chroma signal output of the peak ACC circuit is input to the tuning amp composed of Q001, Q002, L001, L002, C001 and C002. The 688 kHz components are removed here and the frequency components leaking into the AFM band is extracted. This frequency component is clamped by Q003 and is detected and integrated by Q004 for use as the control voltage. V-A conversion of this control voltage is carried out by Q005 and the internal resistance of diode D103 is changed to control the Q of the trap.

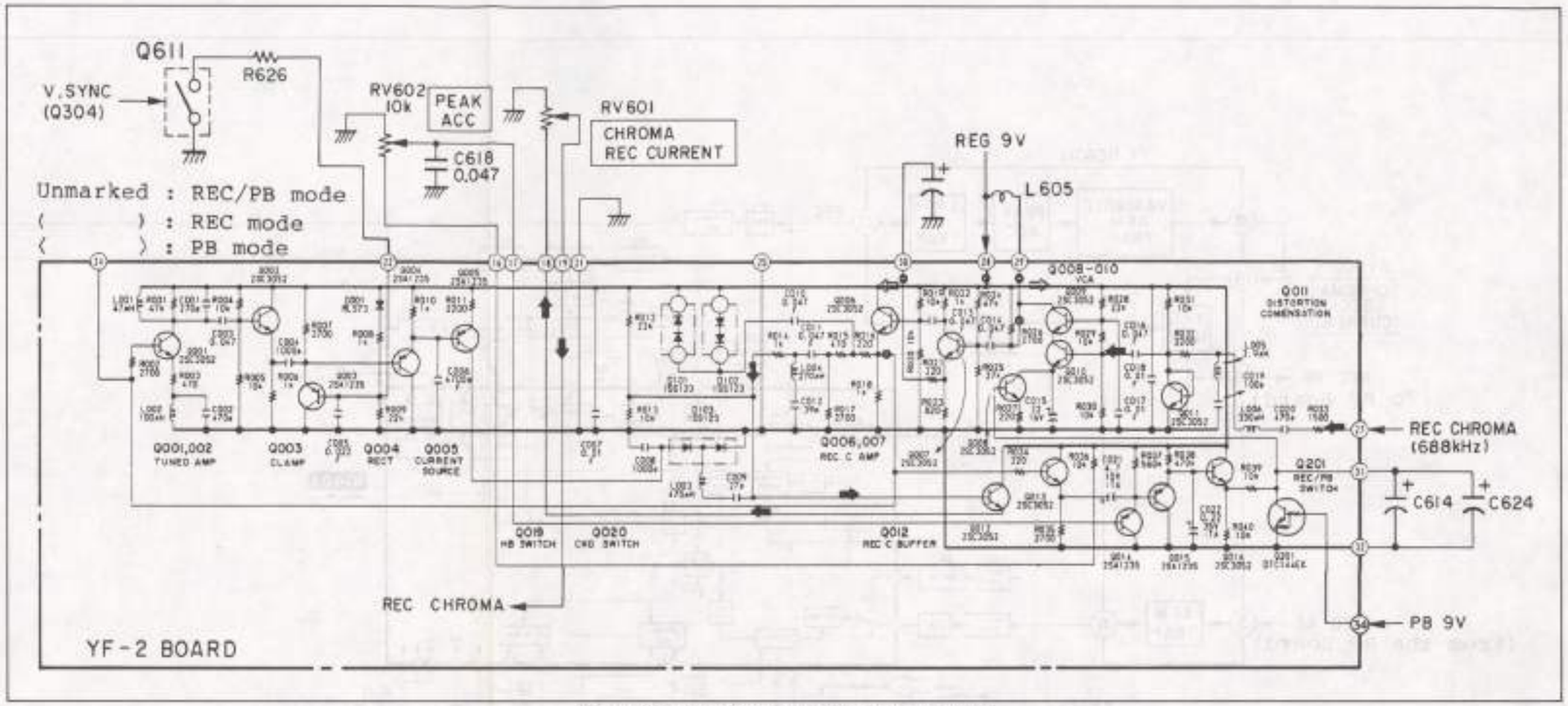


Fig. 1-34 Peak ACC and variable AFM trap circuit

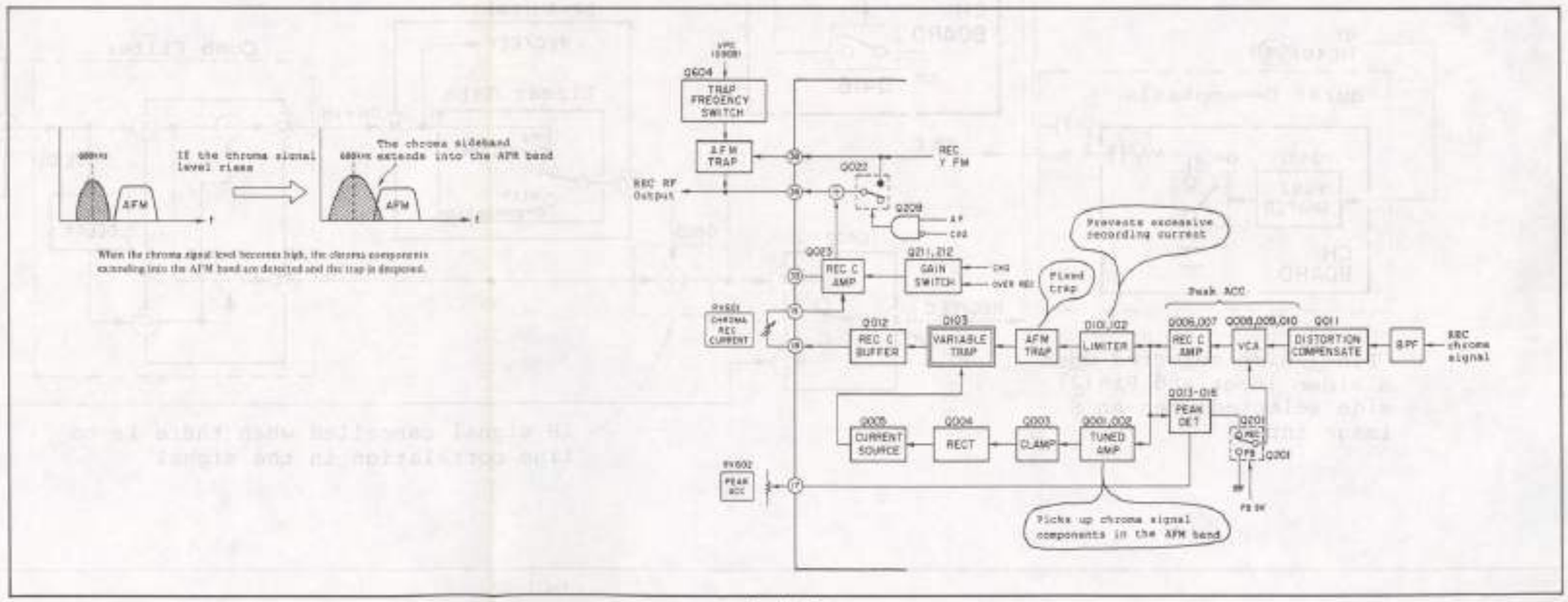


Fig. 1-35

1-4-8. APC Loop of the Playback Mode

The chroma signal converted to 3.58 MHz and 3.58 MHz signal from VXO are compared by APC DET and the VCO oscillation frequency is controlled with the error signal. If the APC loop locks normally, VCO oscillates at 350 fH (5.5 MHz) and this signal is added to CONV I after 1/8 frequency division by the internal counter. A 4.27 MHz signal is generated and the signal enters the PI circuit (phase inversion circuit).

Although playback color is adequately synchronized with the above APC loop alone when color synchronization is operating properly, it does not mean that operation will be stable at all times since the information handled is of burst standard. For example, APC will go into stable locked state as during normal operation even if the burst frequency shifts +/− fH. Because APC alone is unable to correct disturbance, the synchronous system is checked for possible abnormal lock and a correction signal is output from APC-ID (APC group correction) to correct the VCO oscillation frequency. Fig. 1-36 shows the dead zone of APC-ID.

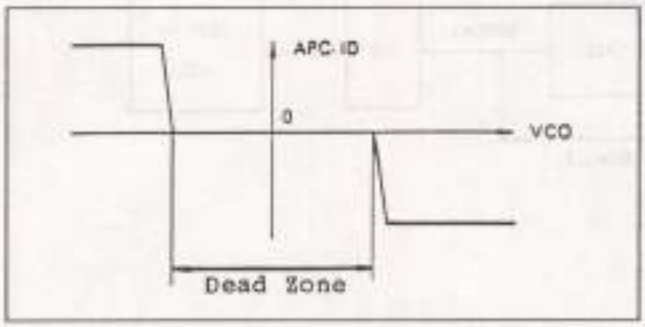


Fig. 1-36 Dead zone of APC-ID

It is necessary that APC-ID operate only when the APC loop is abnormal and be OFF during normal locked state. Also, as long as it is properly locked, it is in normal state even if VCO is disturbed. A dead zone therefore becomes necessary in the APC-ID loop so a dead zone such as shown in Fig. 1-36 is provided. This is to prevent changes of the count of the APC-ID VCO frequency by jitter, etc. since a horizontal sync signal affected by disturbances same as burst is used as the APC-ID gate.

In the case of APC-ID only, APC-ID DET may occur due to crosstalk signals from the effects of the comb filter if the signal contains large amounts of crosstalk components, and HUE disturbance may also occur for several H. BURST is added here and detecting error is prevented by BURST ID DET of the signal after passing the comb filter and convergence is hastened by inverting the phase of the comb filter output and the PB chroma signal.

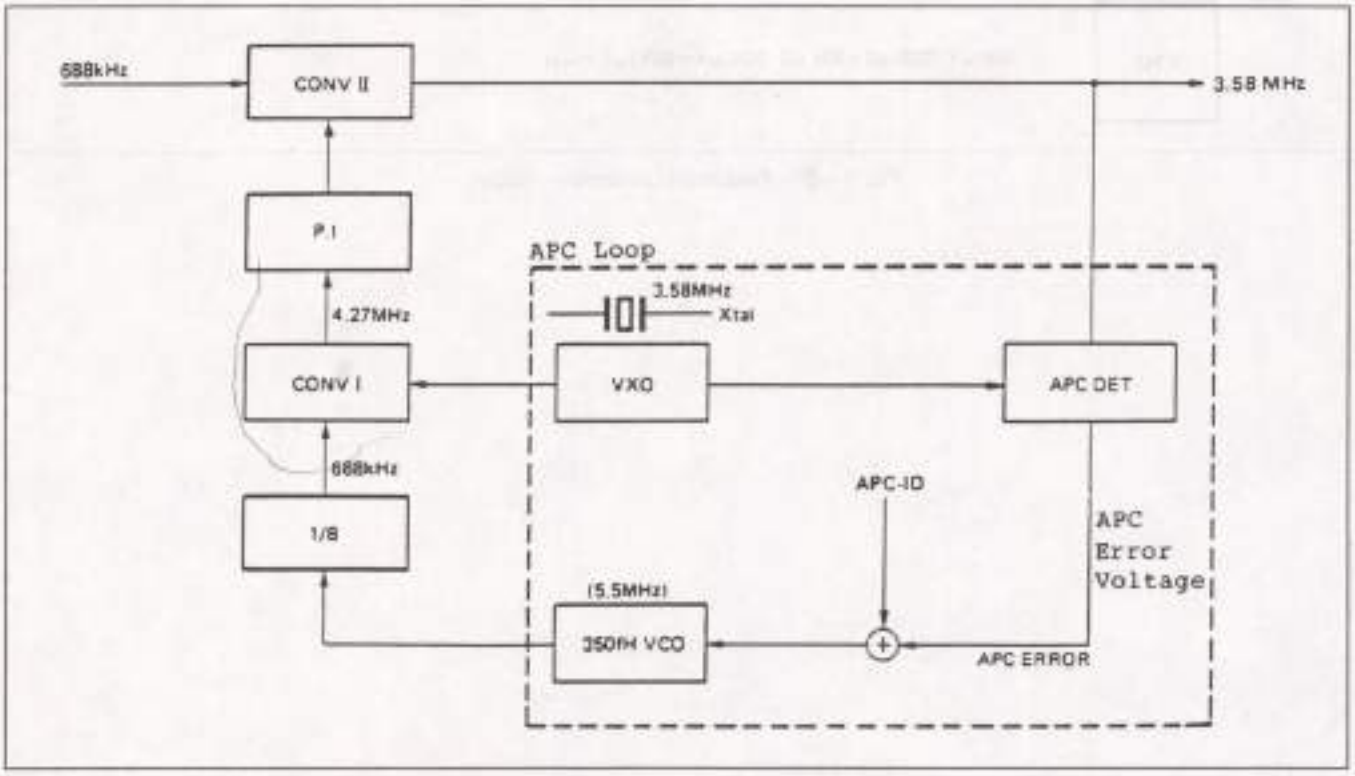


Fig. 1-37 Color method of playback mode.

1-4-9. Frequency Conversion Circuit CONV I (SSB)

A 90° phase shifted signal is created from a 688 kHz signal resulting from a 1/8 frequency division of the VCO output and a 90° phase shifted signal created from the VXO 3.58 MHz signal. These signals are input respectively to two multipliers and the 4.27 MHz USB (UPPER SIDE BAND) extracted by taking the sum of the outputs.

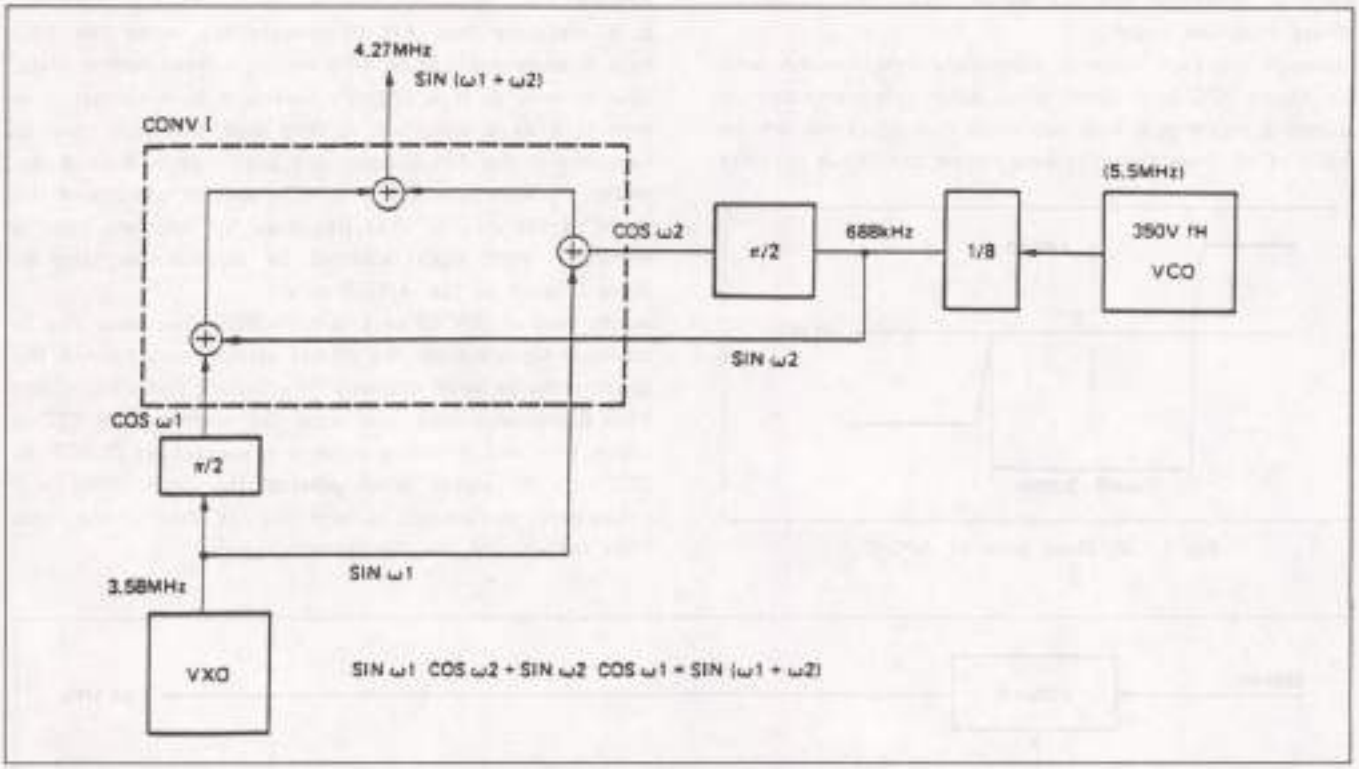


Fig. 1-38 Frequency conversion circuit

1-5. DIGITAL PICTURE CIRCUIT

Purpose

By having the digital picture circuit process video signals during variable speed playback, it is possible to use the video head exclusively for normal playback and thus realize improved picture quality.

The special functions of this digital picture circuit are therefore limited to stop motion and flash motion only.

Although the basic configuration of this circuit is the same as for SL-HF860D, it has become complex since the number of quantized bits has been increased from six to eight to improve picture quality.

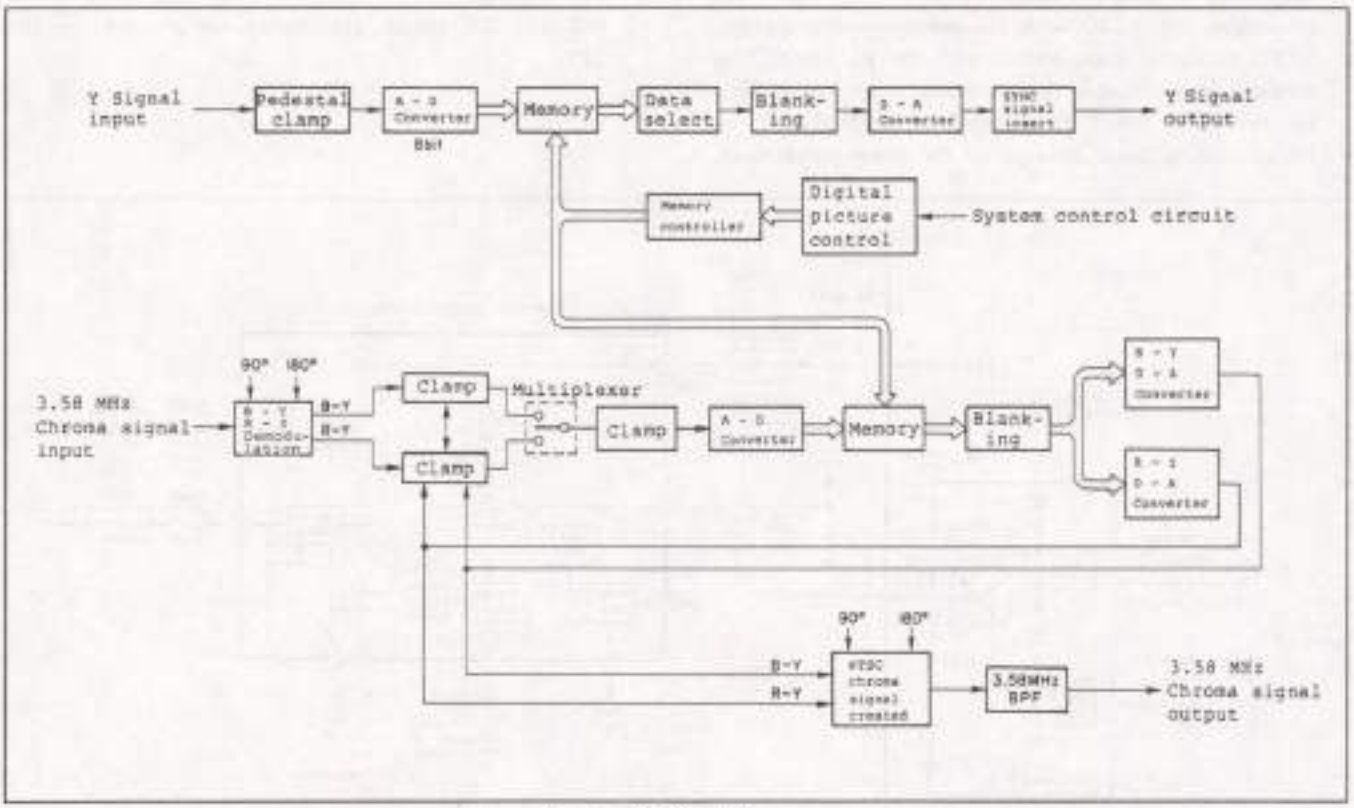


Fig. 1-39 Blockdiagram

1-5-1. Color Difference Signal Demodulating Circuit

Purpose

Demodulates the 3.58 MHz chroma signal and creates the two color difference signals R-Y and B-Y.

Operation

1. The fsc signal (3.58 MHz) from the video circuit is input to Pin ⑤ of IC001 and enters the APC circuit.
2. Two 3.58 MHz demodulating carriers SC90° and SC180° phase locked with the fsc signal are created in the APC circuit. In other words, the 3.58 MHz signal obtained by 1/4 division of the output signal (14.32 MHz) of the 4fsc VCXO (Voltage Control Crystal Oscillator) is phase-compared with the fsc signal. By controlling the VCXO with the resulting error signals, VCXO oscillates phase locked with the fsc signal. The demodulating carrier is therefore also phase locked with the fsc signal. The Y signal input of Pin⑳ of IC001 is for generating burst gate pulses for phase comparison.
3. The chroma signal (3.58 MHz) from the video circuit is input to Pins ⑰ and ⑮ of IC001. The chroma signal burst and the fsc signal are phase locked by the APC circuit of the video circuit.
4. The SC90° and SC180° signals have a 90° phase difference. The chroma signal burst and the SC180° signal are set to the same phase by the voltage on Pin ⑫.

   Therefore, the R-Y signal can be obtained by multiplying the chroma signal and SC90° signal, and the B-Y signal can be obtained by multiplying the chroma signal and the SC180° signal.
5. The residual carrier components of the demodulated R-Y and B-Y signals are respectively removed in the LPF.

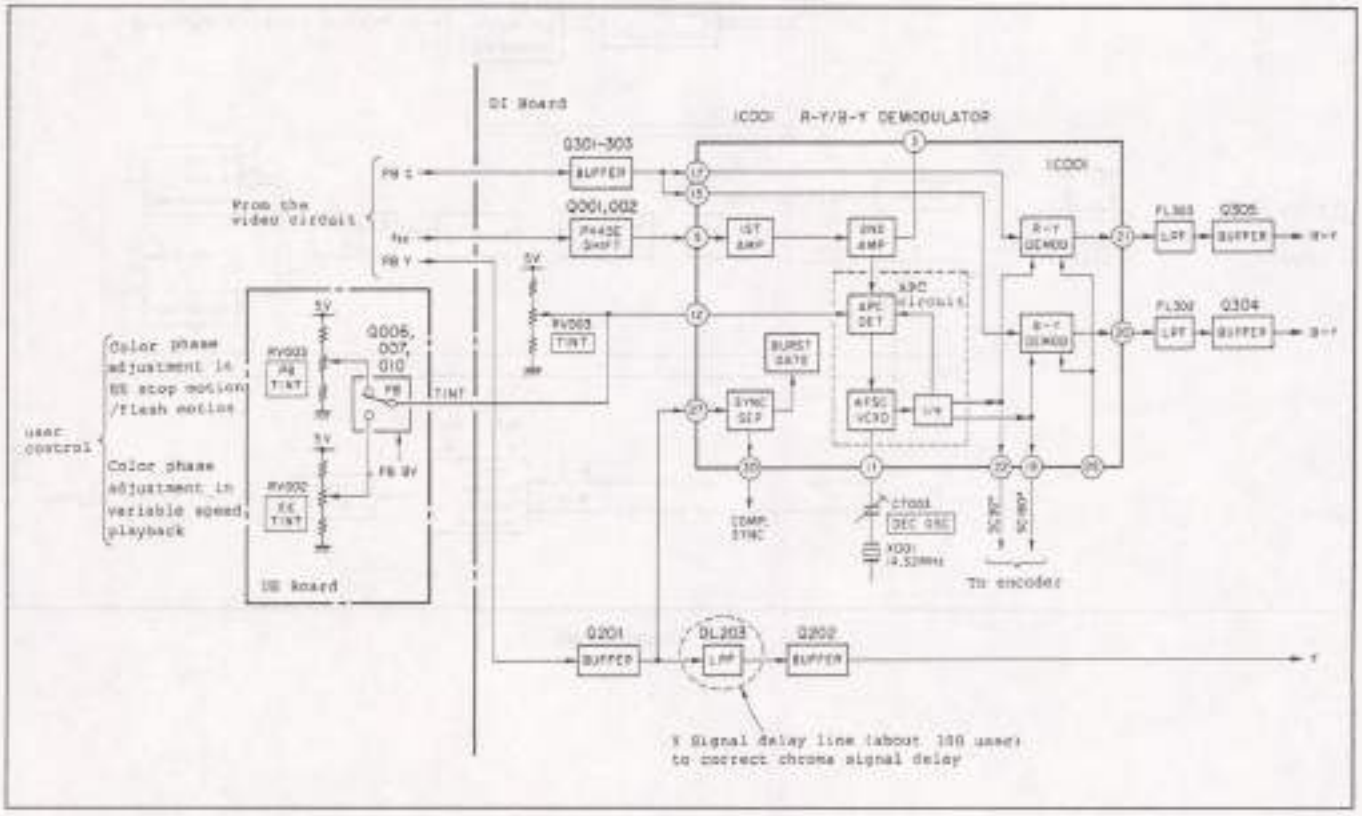


Fig. 1-40

1-5-2. Chroma Signal Multiplexer and Blanking Level Clamp

Purpose

1. Combines the two chroma signals R-Y and B-Y and creates sequential signals R-Y/B-Y.
2. Adjusts blanking level of the R-Y and B-Y signals to the center voltage (VRM = 4 V dc) of the A-D converter.

Operation

1. The B-Y signal is amplified in Q322 and 323 and is input to Pin ① of IC302. Q315 samples the H blanking period voltage of the B-Y signal and holds in C309. This voltge is input to Pin ⑤ of IC301.
2. The R-Y signal is amplified in Q312 and 313 and is input to Pin ⑫ of IC302. Q314 samples the H blanking period voltge of the R-Y signal and inputs it to Pin ⑫ of IC301.
3. IC301 (Pins ① – ③) compares the C309 hold voltage (blanking level of the B-Y voltage) with the blanking level of the R-Y signal and outputs the error voltage to Pin ① and holds.
   The voltage held is fed back to the emitter of Q312. This NF loop therefore serves to equalize the blanking level of the R-Y signal of Pin ⑫ of IC302 and the blanking level of the B-Y signal of Pin ① of IC302.
4. The R-Y and B-Y signals input to Pins ① and ⑫ of IC302 are output alternately every 0.2 μsec from Pin ⑬ by the C MPX signal of Pin ⑩.
5. After clamping the blanking level to VRM (4 V dc) in IC301 (Pins ⑤ – ⑦) of Q324 – 326, this chroma signal is input to chroma A-D converter IC504.

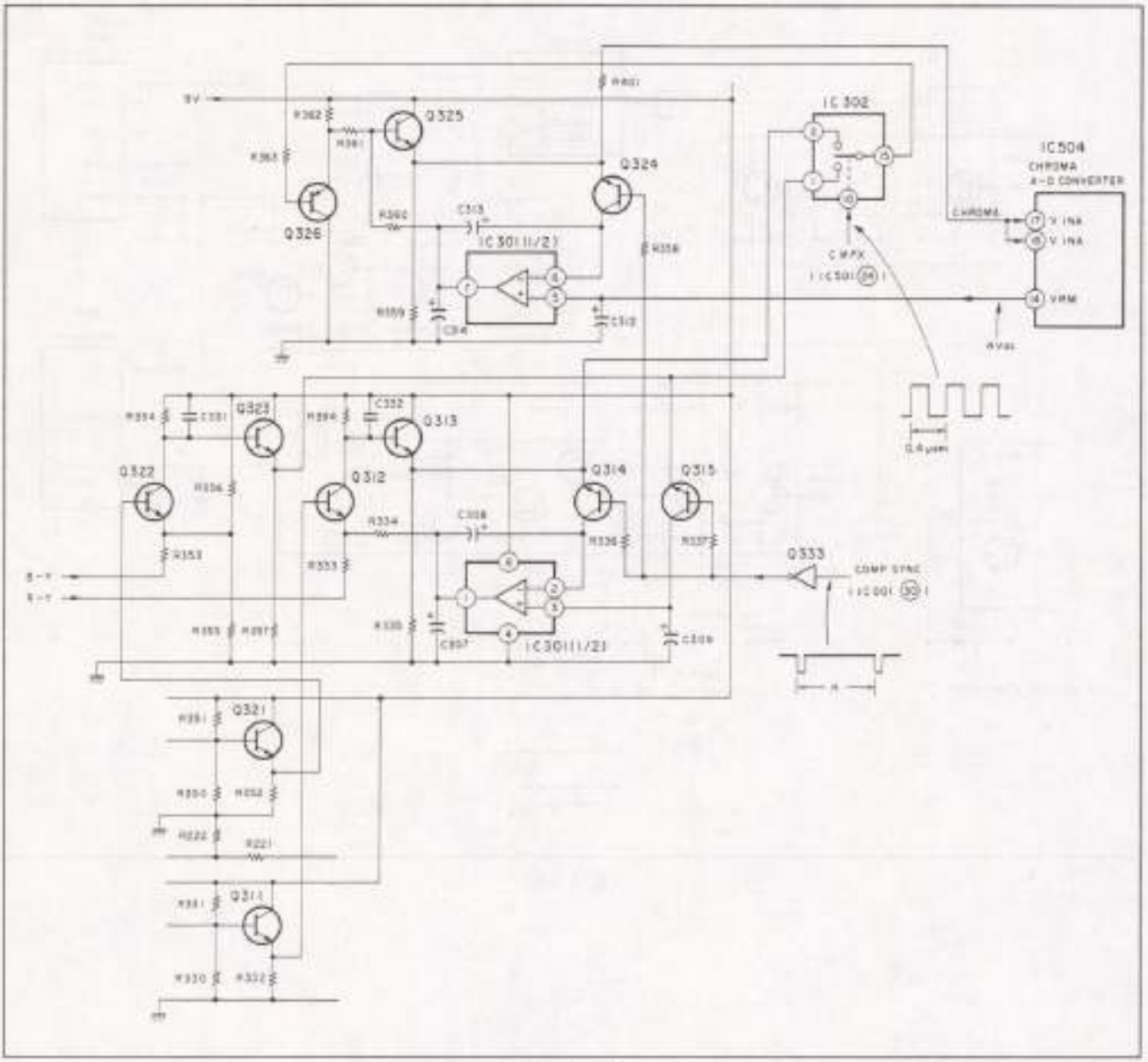


Fig. 1-41

1-5-3. Y Signal Clamp Circuit

Purpose

For effective use of the dynamic range of the A-D converter (8 bit), this unit does not sotre the SYNC signals. For this reason, the pedestal level is clamped with the VRB voltage to match the Y signal pedestal level with VRB (min. voltage = 3 V dc) of the A-D convverter. The Y signal amplitude is also set so the A-D converter dynamic range (VRT − VRB = 2 Vp-p, VRT max. voltage of 5 V dc) will be 80% in the 100% white range.

Operation

1. The Y signal from the video circuit is delayed 300 nsec. in DL203. This is to eliminate color slippage by compensating for delays from chroma signal demodulation.
2. The Y signal is then amplified in Q209 and 210. The Y signal level (amplitude) of the A-D converter input is set by RV201.
3. The pedestal level potential is clamped to the VRB voltage (3 V dc) by Q212 and 213 and the Y signal is input to Pins ⑰ and⑱ of the A-D converter. The VRB voltage is set by RV501, Q501, 502 and 217 serves both as a buffer and temperature compensator.
   The pedestal clamp pulse is created in IC503 by delaying the horizontal SYNC signal HDW separated from the Y signal.

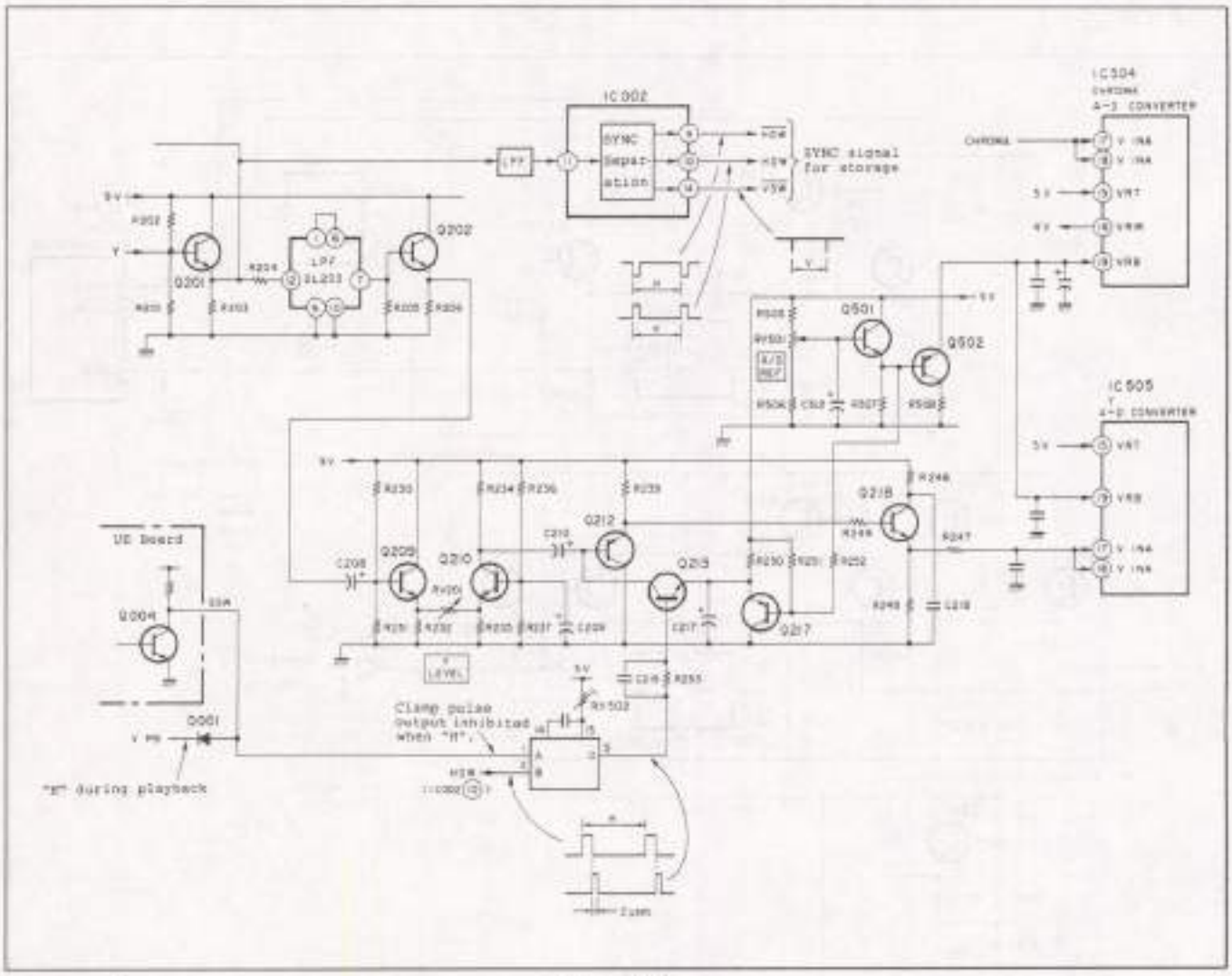


Fig. 1-42

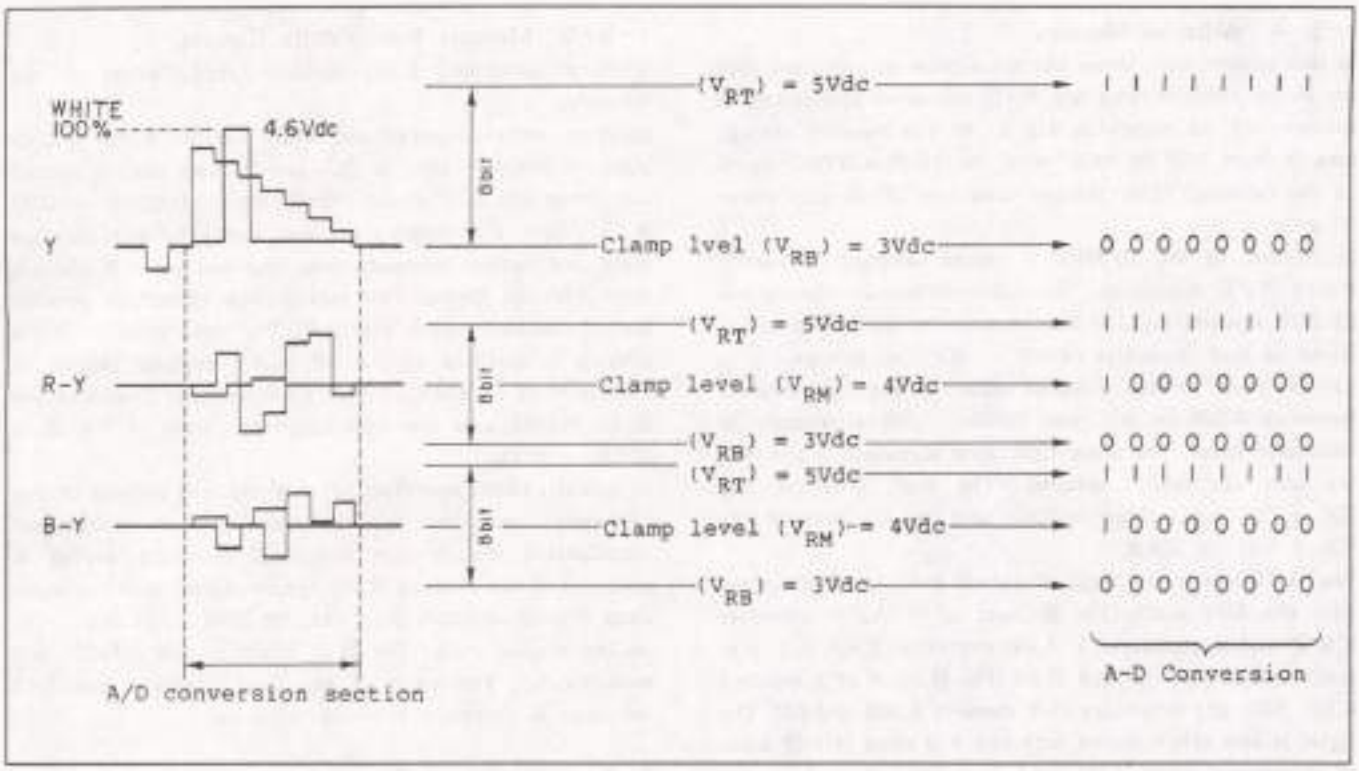

WHITE
100%
4.6Vdc
Y
R-Y
B-Y
A/D conversion section
8bit
8bit
8bit
(V_RT) = 5Vdc
Clamp lvel (V_RB) = 3Vdc
(V_RT) = 5Vdc
Clamp level (V_RM) = 4Vdc
(V_RB) = 3Vdc
(V_RT) = 5Vdc
Clamp level (V_RM) = 4Vdc
(V_RB) = 3Vdc
1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1
1 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1
1 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
A-D Conversion

Fig. 1-43

1-5-4. Write in Memory

In this system, only those picture signals in one field that are in the effective area are A/D converted and stored in the memory. As shown in Fig. 1-44, the memory storage area is from 18H to 240H with the vertical SYNC signal as the reference. The storage area per 1H is also about 50 μsec.

In relation to the 10 MHz Y signal sampling frequency during A/D conversion, the color difference signals are 2.5 MHz respectively. For this reason, the sampled data are stored in four memories (IC506 - 509) as follows.

The Y signal writes sampled data in the two sets of memories IC506 - 507 and IC508 - 509 alternately in successive order. The color difference signals B-Y and R-Y are also alternately sampled. The high order 4 bits (D5 - D8) are written in IC506 and the low order 4 bits (D1 - D4) in IC509.

The A/D converted 8-bit Y signal data is synchronized with the ADY clock (Pin ⑬ input of Y A/D converter IC505) and is output to Y A/D converter IC505. It is also synchronized with the YIA clock (Pin ⑳ input of Y memory IC506, 507) and is written in Y memory IC506 and 507. The signal is also synchronized with the YIB clock (Pin ⑳ input of Y memory IC508, 509) and is written in Y memories IC508 and 509.(See Fig. 1-47) The ADY clock frequency (10 MHz) therefore becomes the sampling frequency of the Y signal. The YIA and YIB clock frequencies are 1/2 the ADY clock frequency (5 MHz) and are 180° out of phase. The 8-bit A/D converted color difference signal is synchronized with the ADC clock (Pin ㉓ input of chroma A/D converter IC504) and is output from chroma A/D converter IC504. The signal is also synchronized with the YIA clock (Pin ㉘ input of chroma memory IC506) and its low order four bits (D5 - D8) are written in chroma memory IC506. It is further synchronized with the YIB clock (Pin㉘ input of chroma memory IC509) and its high order 4 bits (D1 - D4) are written in chroma memory IC509. The sampling frequency of the chroma signal (sequential signals R-Y, B-Y) therefore becomes 5 MHz and the R-Y and B-Y signals 2.5 MHz respectively.

1-5-5. Memory Read/Write Control

Memory controller IC501 controls read/write of the memory.

Memory write is carried out while the $\overline{SIE}$ signal (Pin ⑳ input of IC506 - 504) is "L" and memory read is carried out while the $\overline{SOE}$ signal (Pin ㉒ input of IC506 - 509) is "L". Since this memory is a dual port type with separate input and output terminals, data read and write is possible with different timing. This makes skew correction possible during variable speed playback. The data read or write address is specified by the A0 - A7 language (Inputs of Pins ⑭ - ㉑ of IC506 - 509), CAS language (Input of Pin ㉒ of IC509), and the RAS language (Input of Pin ㉓ of IC506 - 509).

In actual address specification, only the lead address of one horizontal scanning line is specified and subsequent specification during the horizontal scanning period is executed in the memory IC by synchronizing with the input clock (Pin ㉔ of IC506, 507 : YIA, Pin ㉔ of IC508, 509 : YIB) or the output clock (Pin ㉕ of IC506 - 509 : SIO) and counting up. The cycle of the CAS language and RAS language is therefore a horizontal cycle.

1-5-6. Y Signal Data Selector

Since the Y signal data is written alternately in two sets of memories (IC506, 507 and IC508, 509), selection is necessary when reading.

The Y signal data stored in the two sets of memories are selected alternately by IC511 and 512. The selecting signal is Y MPX (Pin ① input of IC511, 512) and is a 5 MHz pulse that becomes "L" when selected on the IC506, 507 side and also "H" when selected on the IC508, 509 side.

1-5-7. Blanking Data Insert Circuit

In this system, only the necessary parts of the Y signal and chroma signal are stored. It is therefore necessary to insert data equivalent to the blanking level during the blanking period (H blanking period and V blanking period). Insertion of the data equivalent to the blanking level is executed by IC513 - 516.

$\overline{SOE}$ (Pin ① input of IC513 - 516) is the switching signal of the blanking data and memory read data. This signal becomes "H" during the blanking period (H and V). The memory read data is selected when the $\overline{SOE}$ signal is "L" and data equivalent to the blanking level is selected when "H". Data equivalent to the blanking level is set by the voltage on Pins ③, ⑥, ⑫ and ⑮ of IC513 - 516 and is "00000000" (4 V dc on Pin ⑥ of IC520) on the Y signal side and "10000000" (4.5 V dc on Pin ⑥ of IC518, 519) on the chroma signal side.

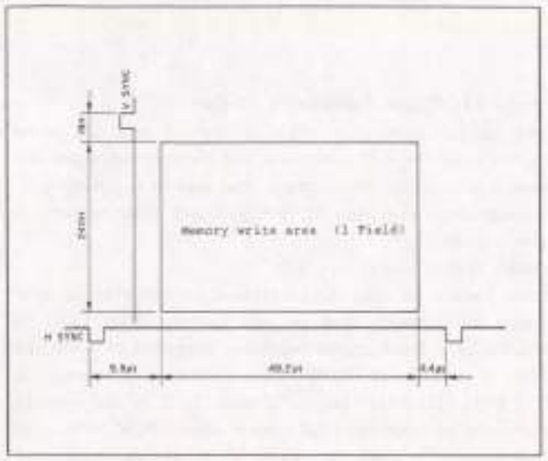


Fig. 1-44

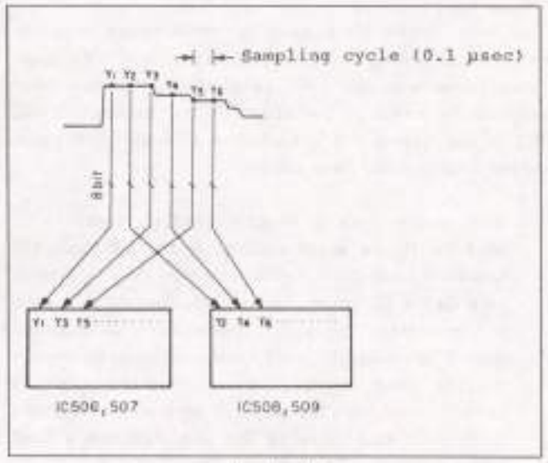


Fig. 1-45

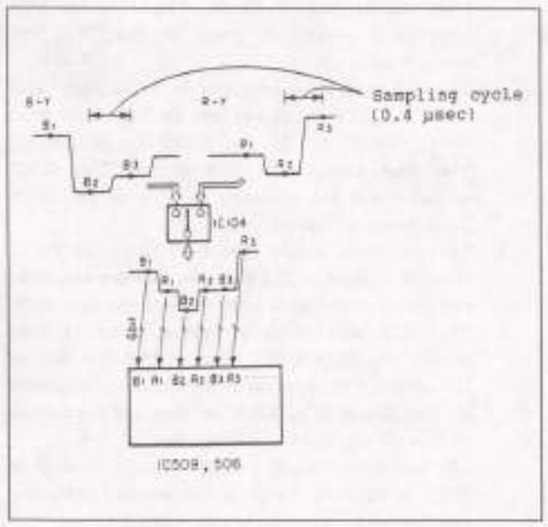


Fig. 1-46

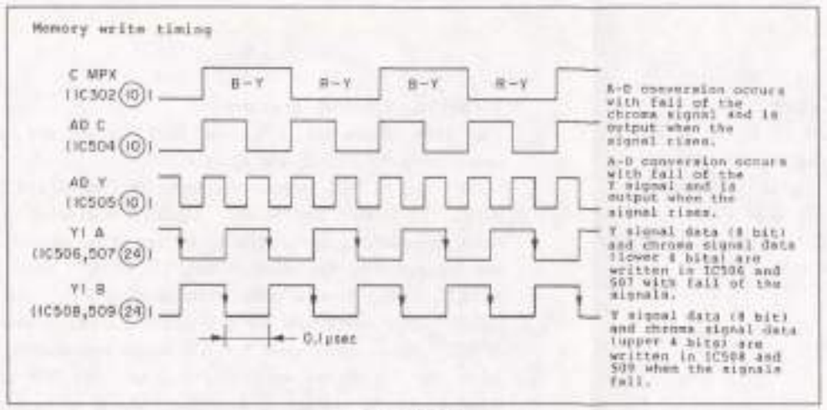


Fig. 1-47

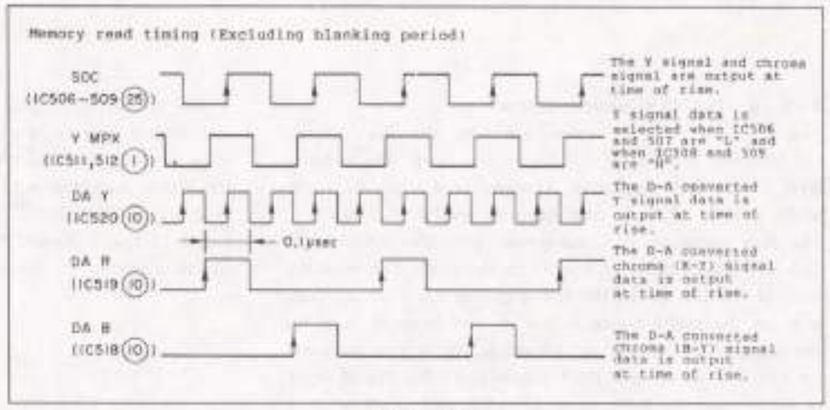


Fig. 1-48

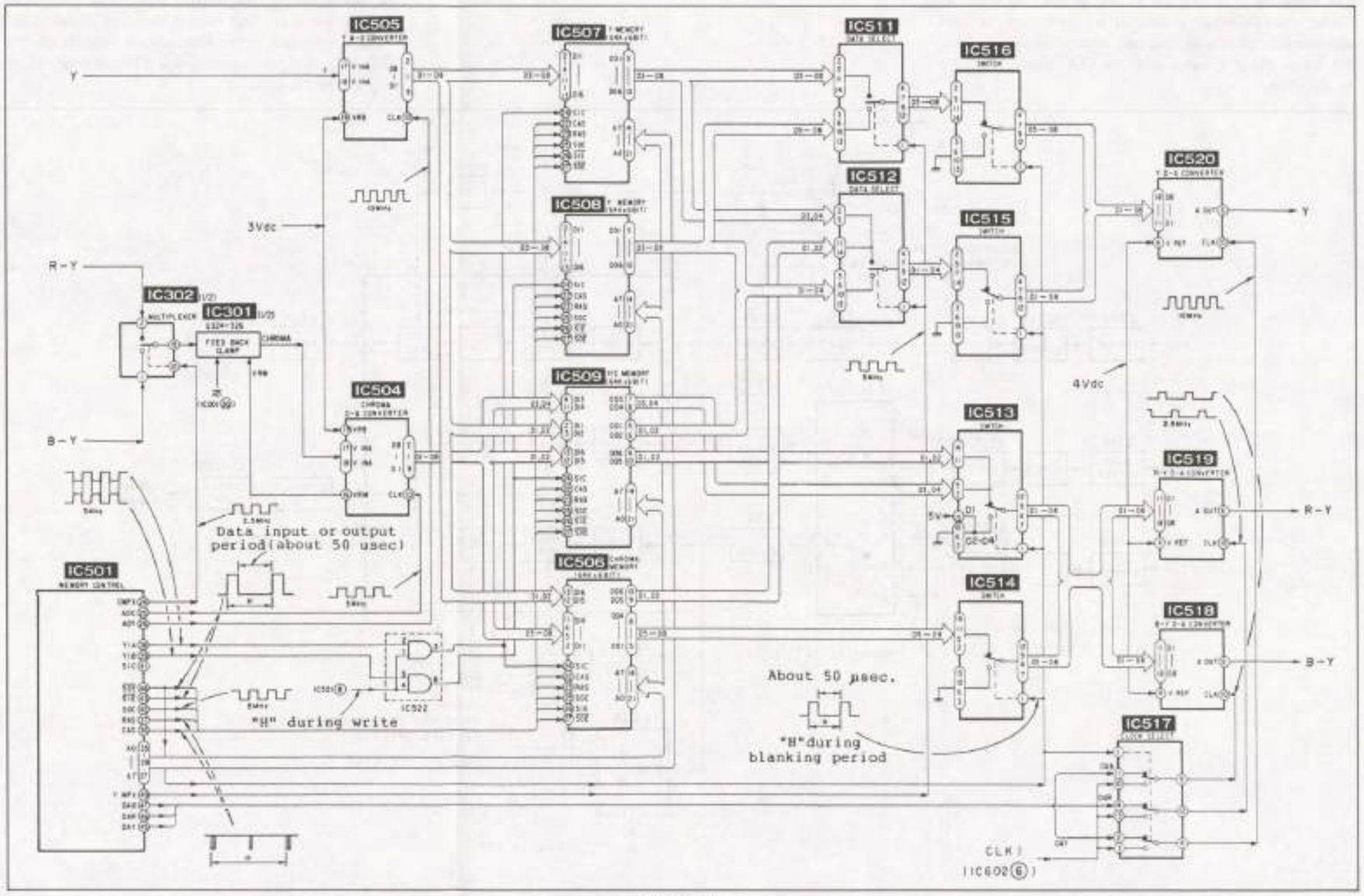


Fig. 1-49

1-5-8. D-A Conversion Circuit

The Y signal is D-A converted with the DAY signal (10 MHz Pin ⑩ input of IC520) as the clock. The pedestal level of the D-A converted Y signal is 4 V dc, its 100% white level is 4.8 V dc and its peak level is 5 V dc.

The R-Y signal is D-A converted with the DAR signal (2.5 MHz Pin ⑱ input of IC519) as the clock. The blanking level of the D-A converted R-Y signal is 4.5 V dc, its peak level on the positive side is 5 V dc and its peak level on the negative side is 4 V dc. Although this is also the same for the B-Y signal, the DAB signal (2.5 MHz Pin ⑩ input of IC518) and the DAR signal are 180° out of phase since the data output timing is different.

The foregoing is in relation to the picture signal period. During the blanking period, D-A conversion of data equivalent to blankig is executed relative to the Y signal, R-Y signal and B-Y signal with the CLK1 signal (20 MHz) as the clock.

1-5-9. SYNC Signal Mixing Circuit

The D-A converted Y signal is input to Pin ⑤ of IC101 after passing through the delay circuit DL202 (800 μsec) for phase matching with the clock signal. The composite sync signal REF SYNC is input to Pin ⑬ of IC151 and is added to the Y signal. The Y signal with the sync signal added is output to the video circuit from Pin ⑭.

1-5-10. Chroma Encoder

The D-A converted R-Y and B-Y signals are input respectively to Pins ① and ⑬ of IC101.

SC90° and SC180° signals are input to Pins ⑰ and ⑳ of IC101. The SC90° and SC180° signals are created in the clock demodulator circuit IC001 and are phase locked with the fsc signal of the video circuit. The SC90° signal and SC180° signal have a phase difference of 90° with the SC90° signal being used for R-Y signal modulation and the SC180° signal being used for B-Y signal modulation.

After the B-Y signal input of Pin ① and the BPF signal input of Pin ③ are mixed, the mixed signal is modulated with the SC180° signal. The R-Y signal input of Pin ⑫ is modulated by the SC90° signal. The two modulated signals are mixed and become the clock signal (3.58 MHz) which are output to the video circuit from Pin ⑭. The BPF signal is a pulse that becomes "H" during the chroma signal burst period.

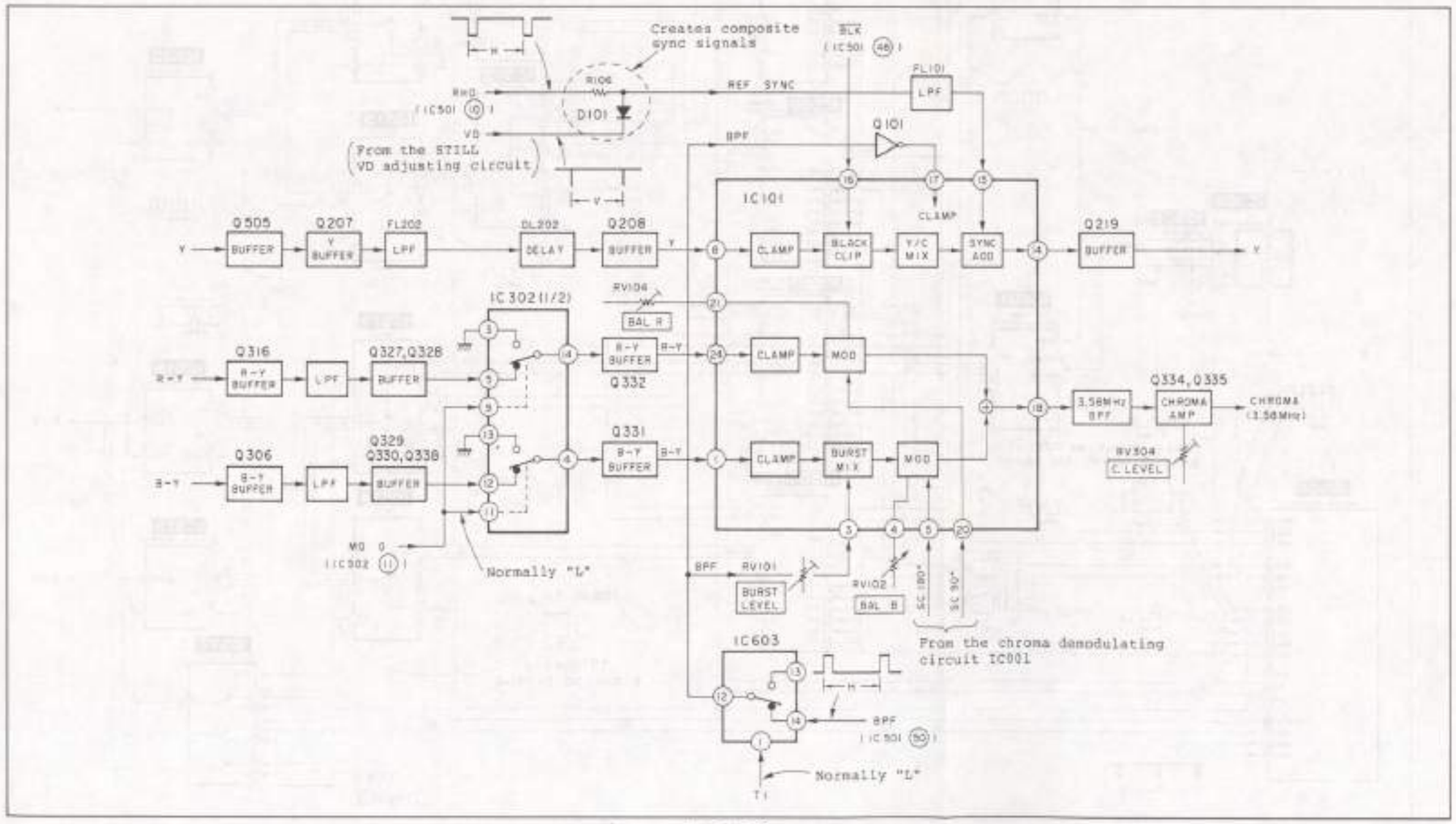


Fig. 1-50

1-5-11. Clock Generating Circuit

The memory controller clock is divided into the write system clock for A-D conversion and memory write and the read system clock for memory read and D-A conversion. Asynchronous operation of the read and write systems is also possible.

(Read System Clock)

Since there is no need to synchronize with an external sync signal for memory read in this system, clock CLK1 is created by a fixed crystal oscillator composed of X601 and Pins ⑤ and ⑥ of IC602. The oscillation frequency is 20.1 MHz (1280 fH) and is divided 1/2 in the memory controller to form the read system clock (10.07 MHz). The D-A conversion clock is created by frequency division of this clock in the memory controller.

(Write System Clock)

The write system clock must be synchronized with the video signal writing in the memory. This clock is therefore synchronized with the $\overline{\text{HDW}}$ signal during variable speed playback by means of the START/STOP oscillator IC605. PLL is also formed and synchronized with the $\overline{\text{HDW}}$ signal during stop motion/flash motion.

(1) Write system clock in variable speed playback

Since the H row is not uniform in the β II mode, the horizontal cycle shifts 1/2H each time there is a track jump during picture search and this appears as a skew on the screen. The write system clock is therefore created by using the start/stop oscillator to prevent this. In other words, the write system clock is resynchronized with the playback horizontal sync signal ($\overline{\text{HDW}}$) for each scanning line and maintains a fixed memory timing relative to the sync signal.

1. The horizontal sync signal ($\overline{\text{HDW}}$) sync separated from the playback Y signal is input to the VCO reset pulse generating circut of Pin ① of the memory controller.
2. The VCO reset pulse generator is synchronized with fall of the $\overline{\text{HDW}}$ signal and sets the VCO reset pulse WHAR (Pin ㊽) to "L" and WHRB (Pin ㊾) to "H". The clock oscillator of Pins ⑥ and ⑦ of IC605 oscillates and the oscillator of Pins ⑩ and ⑪ of IC605 stops oscillating.
3. The oscillation output (about 10 MHz) of Pin ⑦ of IC605 is input to Pin ㊵ of the memory controller and becomes the VCO reset pulse generator clock.
4. The VCO reset pulse generating circuit returns WHRA (Pin ㊽) to "H" and WHRB (Pin ㊾) to "L" about 0.15 μsec later. This causes oscillations on Pins ⑥ and ⑦ of IC605 to stop and oscillations of Pins ⑩ and ⑪ of IC605 to start.
5. The oscillation output (10.07 MHz) of Pin ⑩ of IC602 is input to Pin ㊶ of the memory controller and becomes the write system clock.

(2) Write system clock in stop motion/flash motion

The input signal (Y and clock signals) is stable in Stop Motion and Flash Motion as compared to variable speed playback. The write system clock is therefore synchronized with the input clock by the PLL circuit to prevent following of momentary external disturbances such as noies.

1. The VCO configured of Q603, 604 and D601 oscillates at about 10 MHz and its output is input to Pin ㊴ of memory controller IC501 to become the write system clock.
2. The frequency of the write system clock is divided 1/640 in the memory controller and is output to Pin ㊶ as the WHD signal.
3. The WHD signal is transformed into a trapezoidal wave in the circuit configured of Q601, Q602 and Pins ① – ③ of IC601 and is input to Pin ① of sampling circuit IC604.
4. The horizontal sync signal ($\overline{HDW}$) separated from the Y signal becomes the sampling pulse after short cycle pulses of under 40 μsec is removed and the signal is delayed in IC607. These pulses are then input to Pin ㊶ of IC604. The amount of delay is set by RV601. This determines phase lock of $\overline{HDW}$ and WHD or, in other words, the write timing.
5. The error voltage obtained by sampling the trapezoidal wave is held in C604 and 605 and is fed back to the VCO through Pins ⑤ – ⑦ of buffer amp IC601 to become the VCO control voltage.
6. With the above PLL loop, the VCO oscillates in synchronism with the horizontal sync signal with an oscillation frequency of 640 f_H (10.07 MHz). The horizontal sync signal ($\overline{HDW}$) and the WHD signal will be phase locked.

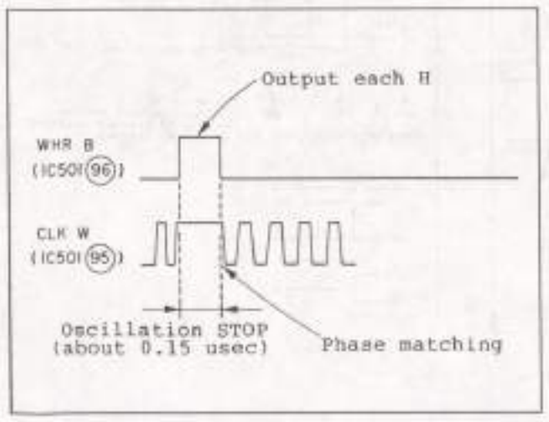


Fig. 1-52

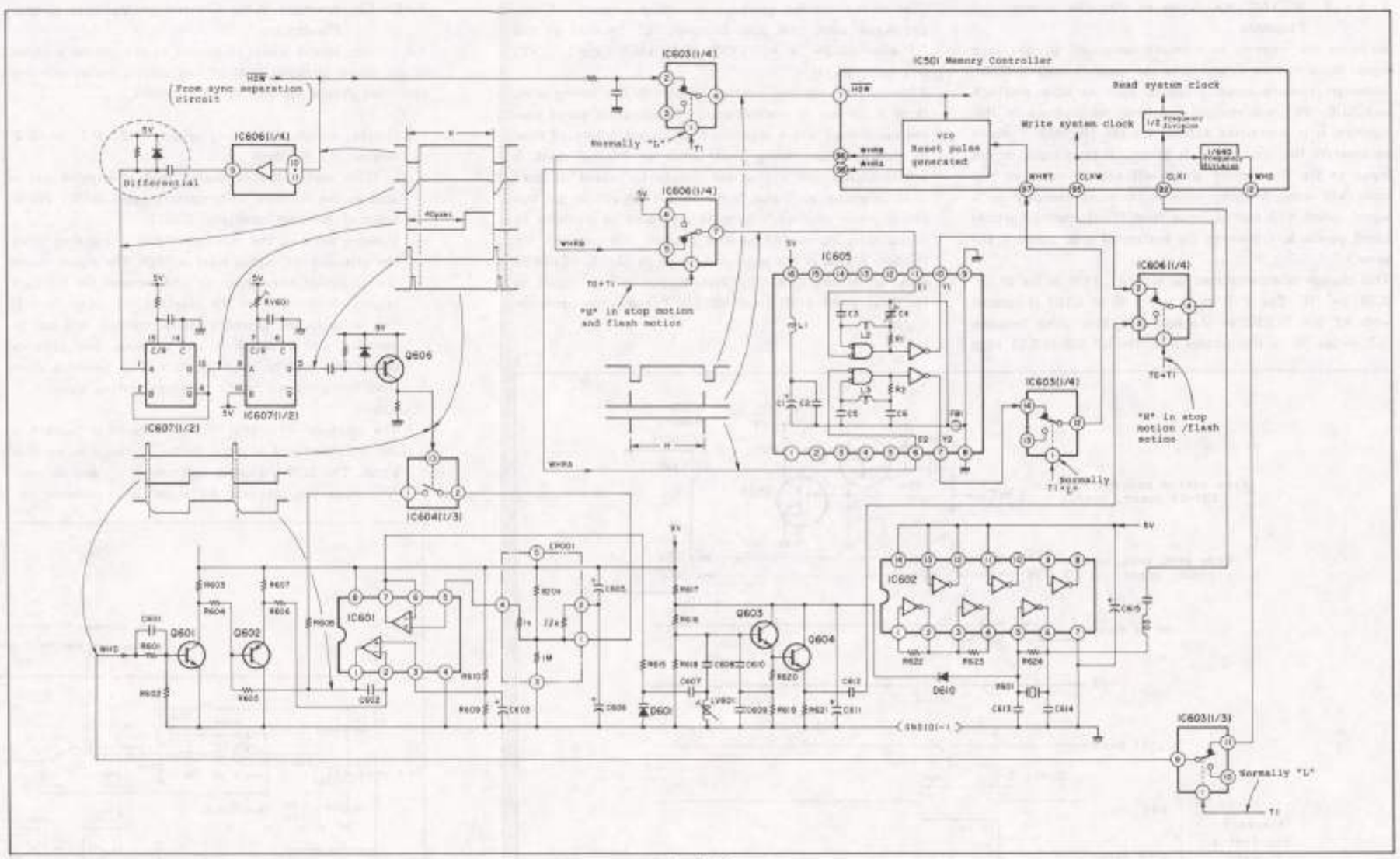


Fig. 1-51

1-5-12. V-SYNC for Write in Variable Speed Playback

Write in the memory is normally controlled by the sync signal input to Pins ① and ② of the memory control IC501. Although variable speed playback such as slow playback and CUE/REV are realized by using the memory in this machine, it is sometimes difficult for the playback Y signal to separate the sync signal. If a vertical sync signal is not input to Pin ②, memory write will not be executed and error will occur. Memory write is therefore executed by a signal called XVS that is input from Pin ⑦ during variable speed playback. (However, the horizontal sync signal is the same.)

This change is accomplished by setting DFSW of Pin ㉒ of IC501 to "H". The XVS input to Pin ⑥ of IC005 is created with RF SW PULSE as the reference. This pulse becomes "L" in the 3H to 10H section from the RF SW PULSE edge (rise or fall) during playback (including forward ×1, ×2) and digital scan. This pulse becomes "L" between 6H and 7H when SLOW or REVERSE PLAYBACK (−×1, −×2) and CUE/REVIEW.

Although the memory control IC detects the falling edge, there is no fear of malfunctioning if operation starts with the initial edge and a separate edge arrives within 12 msec as shown in the timing chart since an internal mask is provided that will not accept inputs for about 12 msec after detecting an input. Input to Pin ⑦ will be by this timing when original V sync is separated in playback or digital scan. Inputs will be at a position 10H from RF SW P when V sync is not separated. When in SLOW, REVERSE PLAYBACK and CUE/REVIEW, signals will be inputs to Pin ⑦ at about a 7H from RF SW P and write operation starts.

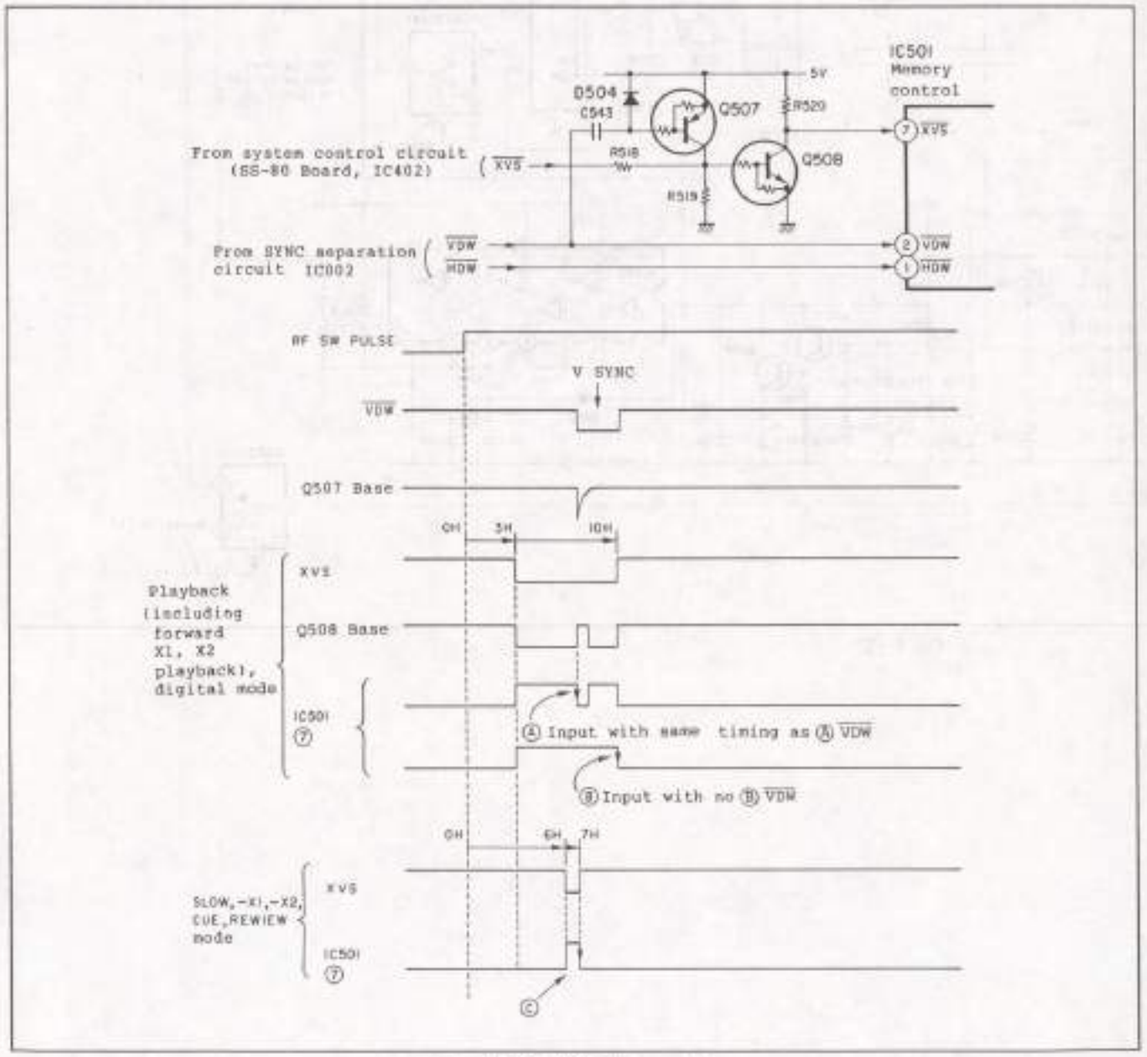


Fig. 1-53 XVS Timing chart

1-5-13. Memory Write Control in Variable Speed Playback

An initially stored signal is output as the playback signal in the digital picture circuit of this unit to realize noiseless operation during variable speed playback.

(1) Picture search, reverse playback ×2, β I or β II reverse ×1 playback

In these modes, the RF signal level is detected and is used as the memory write control signal (SSW: Pin ⑭ input of memory controller IC501).

Memory write of the playback signal is executed when the playback RF signal level is high. The signal stored is read almost simultaneously and becomes the playback output. However, when the playback RF signal level is low, write in the playback signal memory will not be executed and a signal in the previous field or even before this will be read in place. This prevents noise from being output in the playback output signal.

(Operation)

1. The playback RF signal PB RF is envelope-detected in the UE board and is input to the DI board as an SSW signal. The SSW signal is normally "L" and becomes "H" when the playback RF signal level becomes low.
2. When the RF signal level drops and the SSW signal becomes "H", it synchronizes with rise of the HDW signal and Pin ⑮ of IC521 becomes "H". When it synchronizes with rise of the SIE signal, Pin ⑧ of IC521 becomes "L" and Pin ⑨ becomes "H".
3. When Pin ⑭ (SSW) of memory controller IC501 becomes "H" with outputs from Pin ⑨ of IC521, the memory controller write operation is inhibited. When Pins ③ and ⑥ of the AND gate IC522 becomes "L" with outputs from Pin ⑧ of IC521, outputs from the write clock are inhibited. The previously stored data (one field before or further back) remains without being cancelled in this scanning line. This data is read as the compensating signal and becomes the playback output.

The WHSS signal changes the source signal for generating various write timing signals from external input signals such as HDW and VDW to internal controller signals.

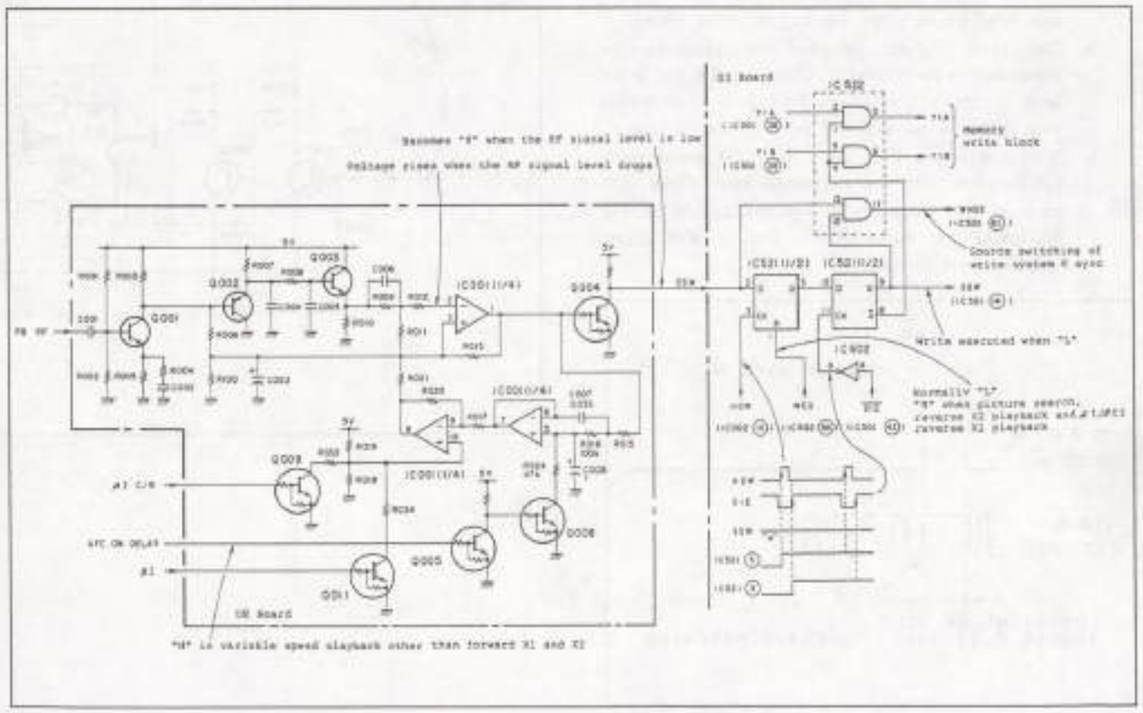


Fig. 1-54

(2) Digital scan and forward ×1 playback

The control signal WE (Pin ⑯ input of memory controller IC801) from the system control is normally "L" in this mode and normal write is executed.

(3) Slow playback, forward ×2 playback and β III reverse playback

Control signal WE from system control is "L" during the period that the Ach head is scanning the track recorded by the Ach head. Write of the playback signal of that track in the memory will be executed. The WE signal is therefore a one field width (16.7 msec) "L" pulse. The pulse cycle will differ with the playback mode.

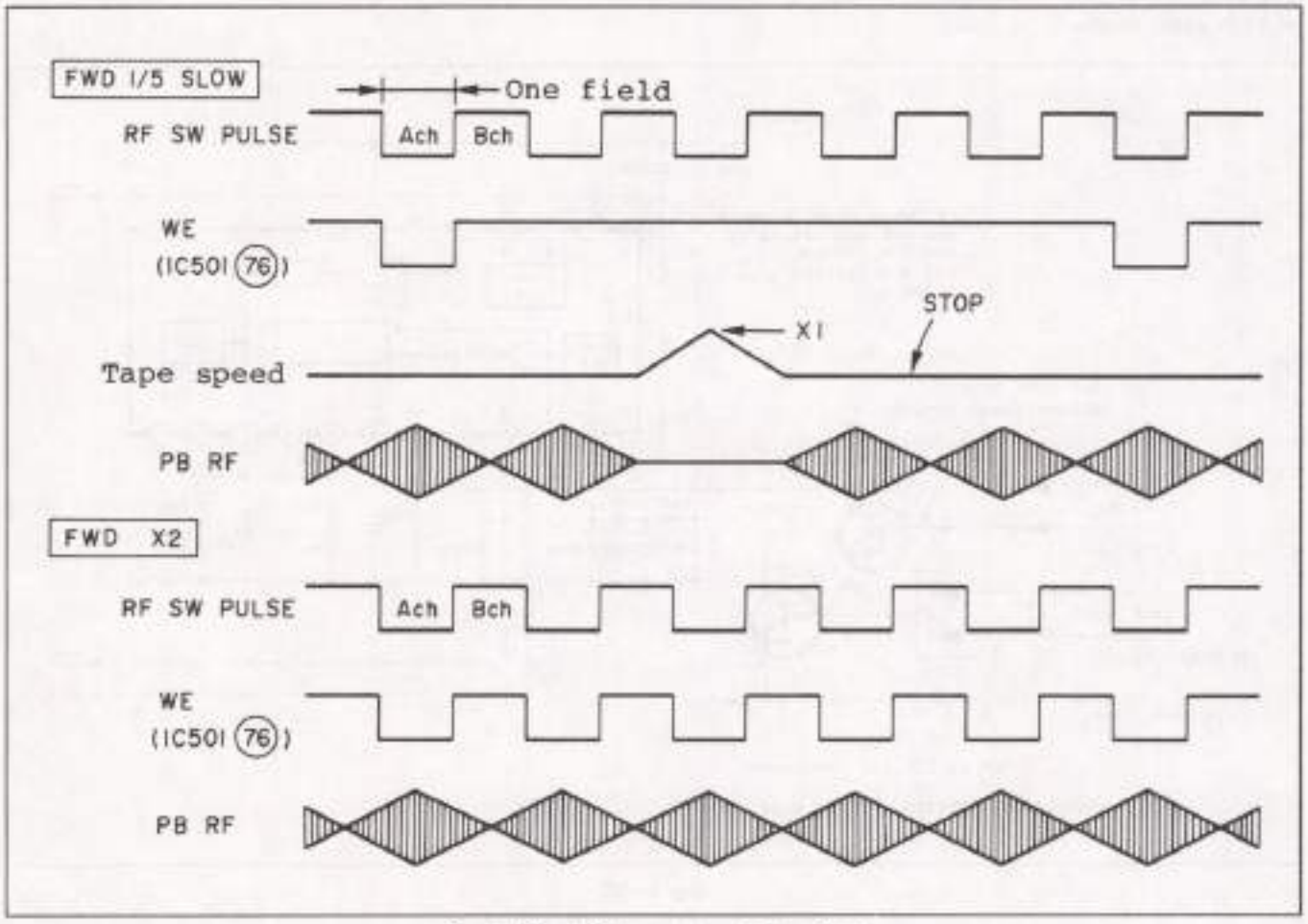


Fig. 1-55 Writing memory timing chart

1-5-14. AFC Circuit

As previously explained, only the effective area of video signal is used in this system and the sync signal is not used. Write in the memory is executed by synchronizing with the sync signal (HDW, VDW) inputs of Pins ① and ⑫ of memory control IC501 and a stable sync signal generated by the controller is added to the signal read from the memory. For this reason, it is not possible to absorb the jitter components, generated when separating the sync signal for write, with the monitor TV AFC. In this unit, PLL is applied to the separated sync signal and is input to the memory controller, (IC002) However, since AFC cannot be applied when writing CUE/REVIEW or $-\times1$, $-\times2$, and digital scan (SSW signal "H") because of the generation of skew, the AFC circuit is jumped by inputting an SSW signal to Pin ⑬ of IC002.

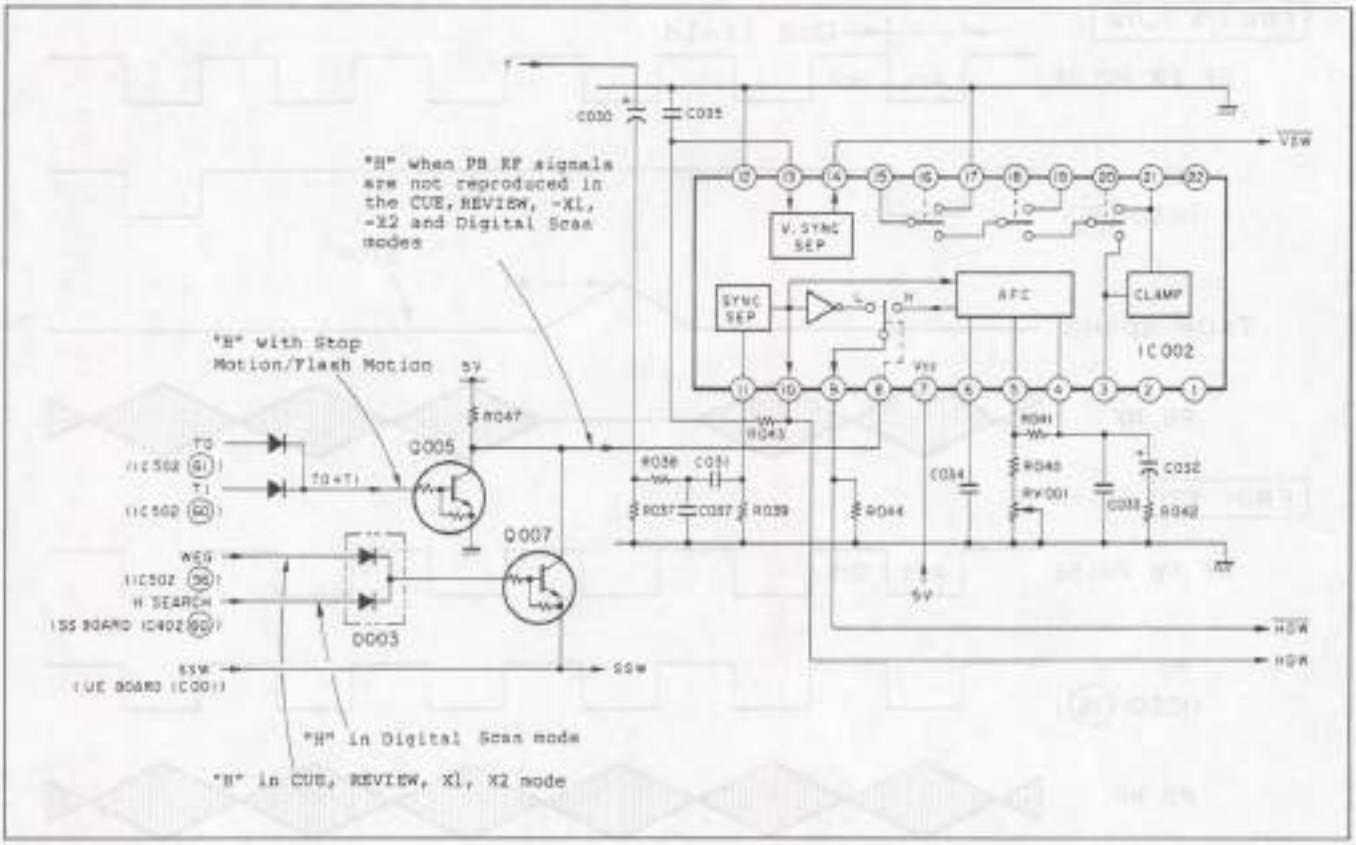


Fig. 1-56

1-5-15. Still Picture Adjusting Circuit

In the Still Picture mode (including stop motion and flash motion), the optimum vertical sync signal inserting position, or the minimum vertical jitter position, differs according to the monitor TV. It is therefore possible to vary the vertical sync signal position of the even numbered fields externally between 0 to 500 μsec with RV501.

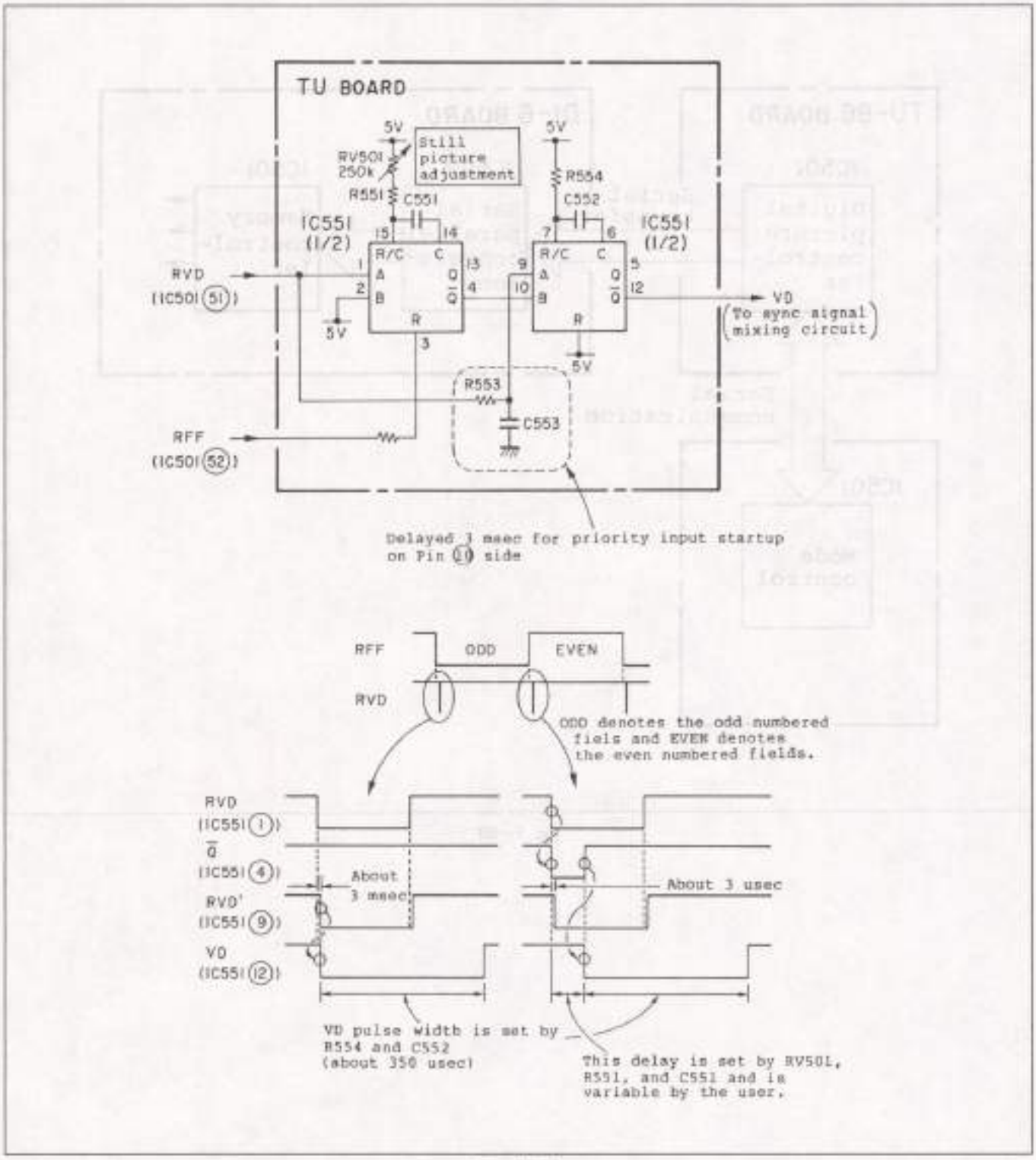


Fig. 1-57

1-5-16. Digital Picture Mode Control

IC501 of board TU-86 controls the digital picture mode. The control signal is serially transferred to IC502 of the DI-6 board along the two lines S OUT (Serial Data Output, IC501 Pin ⑬ output) and SCK (Serial Clock, IC501 Pin ⑭ output). IC502 converts this serial data to parallel data and passes it to memory controller IC501.

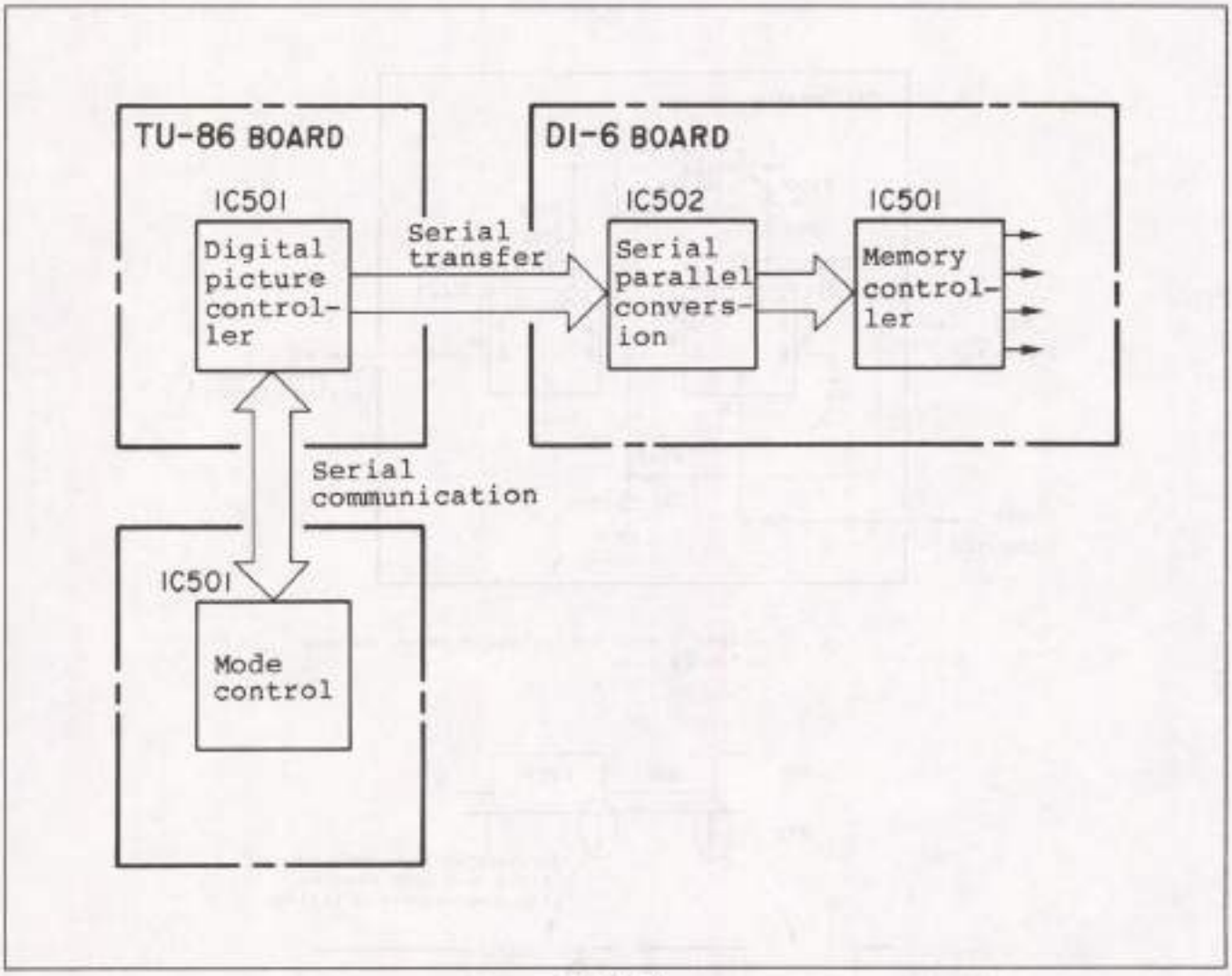


Fig. 1-58

1-5-17. Memory Control IC (IC501) Terminal Functions

Pin No.	Designation	I/O	Logic	Outline	Function
1	$\overline{HDW}$	I	⌐	Write System Horizontal Sync Signal	H Sync input for memory write control signal generation.
2	$\overline{VDW}$	I	⌐	Write System Verticall Sync Signal	V Sync input for memory write control signal generation.
3	N.U				
4	HDR	I	⌐	Read System Horizontal Sync Signal	H Sync input for memory read control signal generation.
5	VDR	I	⌐	Read System Verticall Sync Signal	V Sync input for memory read control signal generation.
6	NVS	I		Reference Signal for VTR Servo	
7	XVS	I	⌐	Vertical Sync Signal Created by RFSWP	V Sync input for variable speed memory write control signal generation.
8	SLTC	O		XVS Position Switching Signal	Not used.
9	SVS	O		Reference Signal Output for VTR Servo	Reference V Sync for servo. Normally synchronized with (NVS). Synchronized with Pin ㊸ (RVD) when variable speed.
10	RHD	O	Negative	Read System Horizontal Sync output	
11	RVF	O	Negative	Read System Equivalent Pulse Period Output	Not used.
12	WHD	O		Read System Horizontal Sync Signal output	Output for write system PLL.
13	FAW	I	Negative	Frame Advanced Write Input	Not used.
14	SSW	I	Negative	Speed Search Write Input	Write control signal by RF signal level detection. "L" when write.
15	DFF	I		Drum FF Input	RF SW Pulse input.
16	VDD	I		+5 V	
17	OKE	I		Test Terminal	"H".
18	T0	I		Clock Mode Switching Terminal	Normally "L", "H" in Stop Motion/ Flash Motion.
19	T1	I			Normally "L".
20	T2	I			Normally "L".
21	TMO	I		Test Terminal	"L"
22	TMO1	O		Read System Horizontal Sync Signal Output	Output for read system clock PLL.
23	TMO0	I		Test Terminal	"L"
24	CMPX	O		Color Difference Multiplex Control Signal	Control Signal for changing over R-Y and B-Y with the analog SW.
25	ADC	O		Chroma System AD Clock	Clock output for alternate A/D conversion of B-Y and R-Y.

Table 1-1 (1)

Pin No.	Designation	I/O	Logic	Outline	Function
26	ADY	O		Y System AD Clock	Clock output for alternate A/D conversion of B-Y and R-Y.
27–35	A7–A0	O		Address Signal	Memory address control output.
36	CAS	O		CAS	Output for memory CAS (Column Address Strobe).
37	RAS	O		RAS	Output for memory RAS (Row Address Strobe).
38	YIA	O	⌐‾	Y System Serial Address Clock	Clock output for fetching A/D converted Y/C data in the memory (IC506, 507).
39	YIB	O	⌐‾	Y System Serial Input Clock	Clock output for fetching A/D converted Y/C data in the memory (IC508, 509).
40	GND	O			
41	SIC	O	⌐‾	C System Serial Input Clock	Not used.
42	SOC	O	⌐‾	Serial Output Clock	Clock output to read data from the memory.
43	$\overline{SIE}$	O	Negative	Serial Input Enable	Memory data input enable signal.
44	$\overline{SOE}$	O	Negative	Serial Output Enable	Memory data output enable signal.
45	DAY	O	⌐‾	Y System DA Clock	Clock output for Y data D/A conversion.
46	DAY	O	⌐‾	R-Y DA Clock	Clock output for R-Y data D/A conversion.
47	DAB	O	⌐‾	B-Y DA Clock	Clock output for B-Y data D/A conversion.
48	BLK	O		Blanking Signal	Read system blanking pulse output.
49	YMPX	O	B/$\overline{A}$	Read System Y Signal Switching Signal	Control pulse to switch data read from two memories and input to D/A converter.
50	BFP	O		Burst Flag Signal	Encoder pulse output to add burst.
51	RVD	O	Negative	Read System Vertical Sync Signal	V sync of read signal.
52	RFF	O	E/$\overline{O}$	Read System Field Discrimination Output	Odd field with "L".
53	N.U	O			
54	WFF	O	E/$\overline{O}$	Write System Field Discrimination Output	Odd field with "L".
55	WVD	O	Negative	Write System Vertical Sync Output	V sync output created by the internal write counter. Synchronizes data communications with IC502.
56	MO0	I		Expansion Multiple Specification M	Not used.
57	MO1	I		Expansion Multiple Specification M	

Table 1–1 (2)

Pin No.	Designation	I/O	Logic	Outline	Function
58	MO2	I		PIP Position Specification M	Not used.
59	MO3	I		PIP Position Specification M	
60	MO4	I		Mosaic Level Specification M	Not used.
61	MO5	I		Mosaic Level Specification M	
62	MO7	I		Test Terminal M	"L".
63	REH	I	Positive	Memory Output Enable M	"H".
64	RVS	I		Read System Sync Control M	Switches memory read system to synchronization with each section or to free run. "L" when external sync.
65	VDD			+5 V	
66	WHVD	I		Read System Write Sync Control M	"H".
67	DFSR	I		Read System V Sync Source Changeover M	
68	SWH	I		Memory – Slew Image Switch M	Memory image/slew image control signal input.
69	GSEL	I		Frame Indication ON/OFF M	"L".
70	RR	I	Negative	Read System Reset	"L" when reset.
71	MO6	I		PIP ON/OFF M	"L".
72	M10	I		Reduction Rate specification (V Direction) M	Not used.
73	M11	I		Reduction Rate specification (V Direction) M	
74	M12	I		Reduction Rate specification (H Direction) M	Not used.
75	M13	I		Reduction Rate specification (H Direction) M	
76	WE	I	Negative	Write Enable M	Memory write enable signal output. "L" when writing with system control.
77	WEG	I		Write Enable Source Changeover M	
78	N.U			NC Terminal	
79	WES	I		Special Rewrite Enable Changeove M	"H"
80	WHSG	I		Write System H Sync Source M	
81	WHSS	I		Write System H Sync Switching Control M	
82	DESW	I		Write System V Sync Source Changeover M	Switching control signal of V sync for write.
83	SLH	I		Slow Mode Signal M	Not used.
84	SVC	I		Servo System V Sync Source Changeover M	Control input taht switches SVS output of Pin ⑨

Table 1-1 (3)

Pin No.	Designation	I/O	Logic	Outline	Function
85	WR	I	Negative	Write System Reset	"L" when reset.
86	DATA	I		Serial Data M	Transfers memory write, read start address data serially from IC502.
87	SCK	I		Serial Clock M	
88	DWDR	I		Serial Data Changeover M	
89	TEST	I		Test Terminal	"L".
90	MTSC	I		PAL-NTSC Changeover	"L" when NTSC
91	GND				
92	CLKI	I		Read Clock Input	1280 f Clock input. Becomes 640 f with internal frequency division.
93	CLKO	O		Read Clock Output	
94	XIE	I		Test Terminal	"L"
95	CLKW	I		Write Clock Input	640 f Write System Clock input.
96	WHRB	O		CLKW Enable	"L" when write system clock VCO oscillating.
97	WHRT	I		VCO Resetting Clock	Clock input for genetating write system clock VCO reset pulses.
98	WHRA	O		WHRT Enable ($\overline{\text{WHRB}}$)	"L" when resetting write system clock VCO.
99	WG	O	Positive	Frame Signal	Not used.
100	SWMM	O		Memory-Slew Switching Output	Memory image when "H".

Table 1-1 (4)

2. SYSTEM CONTROL CIRCUIT

Centering the mode control microcomputer on the MO-5 board, the system control circuit is composed of the circuits as shown below.

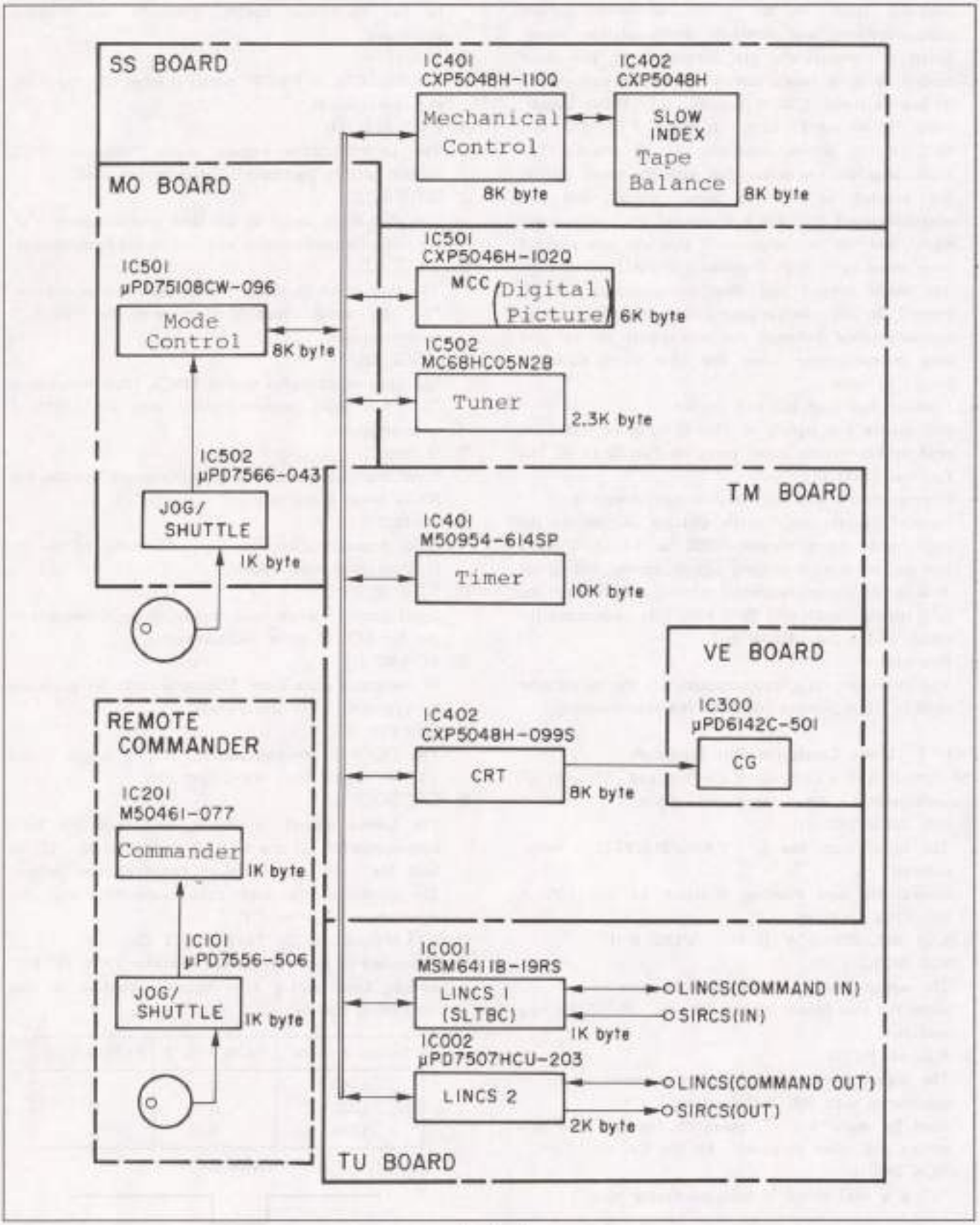


Fig. 2-1

2-1. MODE CONTROL MICROCOMPUTER

The mode control microcomputer has the following principal functions.

- Communication bus control
  The MO-5 board mode control microcomputer IC501 positions itself in the center of microcomputer communications and controls communication buses. Seven microcomputers are connected to the mode control by serial buses, namely, mechanical control (SS-80 board), timer (TM-92 board), CRT (TM-92 board), tuner (TU-86 board), LINCS 1, LINCS 2 (TU-86) and MCC (digital picture controller TU-86 board). The microcomputers communicating with the mode control are selected by a chip select signal, and the microcomputers that are not selected by a chip select signal, and the microcomputers that are not selected have buses open (high impedance status).
  The mode control and slow microcomputer (SS-80 board) do not communicate directly. Communications are established between the mechanical control and slow microcomputer when the chip select signal is output to them.
- Function key read out and display
  Key matrix out signals of Pins ㉗ to ㉚ of IC501 are read at key matrix input ports on Pins ㉘ to ㉛. The function LEDs lit.
- Communication with jog/shuttle microcomputer
  Signals from the jog/shuttle dial are decoded by the jog/shuttle microcomputer IC502 on the MO-5 board and are converted into three signals, namely, roll speeds A, B and C. The mode control receives data through the J/S request signals (Pin ㉜ of IC501) to understand the status of the jog/shuttle dial.
- Edit control
  The mode control microcomputers on the player and recorder sides control assemble and insert editing.

2-1-1. Mode Controller Pin Function

The numberals in a circle show Pin Nos. and "I" and "O" in parentheses ( ) show input and output.

① ROL DIRECTION (I)
The signal from the J/S (JOG/SHUTTLE) microcomputer.
Shows the tape running direction by the JOG / SHUTTLE operation.

④, ③, ② ROL SPEED A (I), ROL SPEED B (I), ROL SPEED C (I)
The signals from the J/S microcomputer.
Show the play speeds by the JOG dial/SHUTTLE ring operation.

⑤ ROL PULSE (I)
The signal from the J/S microcomputer (pulse in accordance with JOG dial rotation).
Used by the "+/−" operation (channel and title setting and other purposes) by the JOG dial.

⑥ $\overline{\text{MON IND}}$ (I)
"L" if a HiFi signal is detected during play.
Used by audio monitor selection processing.

⑧ $\overline{\text{SLOW CTL}}$ (I)
This is the tape counter correction signal input.
"L" for SLOW play.

⑨ TOP/$\overline{\text{END}}$ (I)
The signal to show the tape feeding direction supplied by the mechanical control. Used by tape counter processing.

⑩ CTL (I)
The REC CTL or PB CTL signal is input. The input for the tape counter.

⑪ EXIT REQ (O)
The communication request signal from the MCC (digital picture controller). Currently not used.

⑫ $\overline{\text{SLOW-CS}}$ (O)
The chip select signal to the slow microcomputer. "L" for serial communications with the slow microcomputer.

⑬ $\overline{\text{LI2-CS}}$ (O)
The chip select signal to the LINCS 2 microcomputer. "L" for serial communications with the LINCS 2 microcomputer.

⑭ $\overline{\text{LI1-CS}}$ (O)
The chip select signal to the LINCS 1 microcomputer. "L" for serial communications with the LINCS 1 microcomputer.

⑮ SI BUS (I)
Serial communication data input. Connected to the Pin SO of other microcomputer.

⑯ SO BUS (O)
Serial communication data input. Connected to the Pin SI of other microcomputer.

⑰ $\overline{\text{SCLK}}$ (I/O)
Serial communication clock input/output. Connected to the Pin SCK of other microcomputer.

⑱ RF SWP (I)
RF switching pulse input. The mode controller processes by syncronizing to this signal.

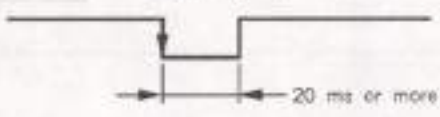
⑲ TV/VTR (O)
The TV/VTR selection output. "H" for output of the VTR RF signal from the output Pin.

㉒ $\overline{\text{J/S RQST}}$ (O)
The timing output to receive data from the J/S microcomputer. Set the level of this signal to "L" to hold the J/S microcomputer communication output. The mode controller reads data during the rise of this signal from "L" to "H".

㉓, ㉔ TAPE SEL Ⅱ (I), TAPE SEL Ⅰ (I)
Connected to the tape balance indicator TAPE SELECT switch. Used during tape balance counting by the mechanical control.

Switch Position	TAPE SEL Ⅰ	TAPE SEL Ⅱ
L500	H	H
L750	L	H
L830	H	L

Table 2-1



㉕ CAM PAUSE IN (I)
The camera pause input. Effective during the REC or REC PAUSE mode. The mode shifts REC ⇄ REC PAUSE for each input of a pulse.

㉖ JOG/SHUTTLE (I)
A signal from the J/S microcomputer. "H" for shuttle operation.

㉗ to ㉚ KEY OUT 0 to 3 (O)
Key scanning output. Normally all active ("L"). Press the key to output a key scanning oulse.

㉛ to ㉞ MKMI 0 to 7 (I)
Key scanning input. MKMI 7 is not used.

㉟ MECH-CS (O)
The chip select signal to the mechanical control. "L" for serial communications with the mechanical control.

㊱ TIMER-CS (O)
The chip select signal to the timer microcomputer. Also input to the CRT microcomputer. "L" for serial communications with the timer microcomputer. The output data from the mode control at this time is transfered to the CRT microcomputer also.

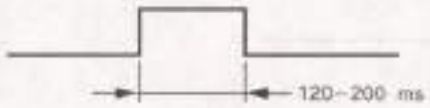
㊲ TUNER-CS (O)
The chip select signal to the tuner microcomputer. "L" for serial communications with the tuner microcomputer.

㊳ MCC CS (O)
The chip select signal to the MCC (digital picture controller). Also input to the timer and CRT microcomputers. "L" for communications with the MMC.

㊴ RESET (I)
The system reset input from the timer microcomputer. "L" for resetting.

㊵, ㊶ 4.19 MHz clocks.

㊷ LINCS 2 READY
The communication request signal from the LINCS 2 microcomputer. "L" if communication request is received.



㊸ CAM PAUSE OUT (O)
The camera pause output for editing. "H" pulse is output when shifting the mode of the VTR on the recording side REC → REC PAUSE.

㊹ STEP (I)
The step feed signal from the mechanical control. Used to correct the counter during the slow and frame feed play modes.

㊺ HI-BAND (O)
SUPER BETA on-off output. "H" for the SUPER BETA mode.

㊻ EDIT CONT (O)
The "EDIT" LED drive port. "L" for lighting.

㊼ β HiFi REC (O)
BETA HiFi REC control output. "H" for BETA HiFi record mode.

㊽ PAUSE LED (O)
The "PAUSE (⏸ ⏭)" LED drive port. "L" for lighting.

㊾ VTR LED (O)
The "VTR" LED drive port. "L" for lighting.

㊿ REW LED (O)
The "REW (◀◀)" LED drive port. "L" for lighting.

(51) FF LED (O)
The "FF (▶▶)" LED drive port. "L" for lighting.

(52) PB LED (O)
The "PB (▶)" LED drive port. "L" for lighting.

2-1-2. Data Bus Communications

(1) Data bus communication timing

Communications are activated between the mode controller and microcomputers through internal buses (serial) once per field in the order of LINCS 1 (IC001 on the TU-86 board), mechanical control (IC401 on the SS-80 board), timer/CRT (IC401/402 on the TM-92 board), tuner (IC802 on the TU-86 board) and MCC (digital picture controller, IC501 on the TU-86 board). Communications with the LINCS 2 microcomputer (IC002 on the TU-86 board) are activated anytime by interrupting communications with the other microcomputers when a communication request port (Pin 42 of the mode controller : LINCS 2 RDY) is checked immediately before starting communication with the timer/CRT microcomputer. If the level is "L", communications with the LINCS 2 microcomputer are excuted first.

The mode controller outputs "L" to the matching CS port depending on the communication timing with each microcomputer to notify that the serial data matches the microcomputer. The level of $\overline{\text{TIMER-CS}}$ sometimes becomes "L" is for direct communications from the timer microcomputer to the CRT microcomputer without passing through the mode controller, and communications from the timer to the CRT are activated if both $\overline{\text{TIMER-CS}}$ and $\overline{\text{MCC-CS}}$ are "L". Therefore, the CRT microcomputer receives $\overline{\text{TIMER-CS}}$ and $\overline{\text{MCC-CS}}$ as chip select signals to it and distinguishes data received from the mode controller and timer in accordance with the category codes of the received data.

To avoid a confusion in mode controller processing caused by noise or by other reasons, communications with the LINCS 2 microcomputer are limited to less than once till the CRT microcomputer communication timing is received and to than once (maximum twice per field) before entering the next field thereafter. (Normally, mode controller processing and the LINCS signal output by the other set connected to control T are not synchronized, and a maximum two communications are needed per field.)

All main processing is finished in 15.6 ms after the start of the field, the next field starts by synchronizing to the edge of RF SW PULSE if communications with the LINCS 2 microcomputer are not activated.

If the RF SW PULSE edge is not input in 18 ms, however, all main processing is finished, and the next field starts unless communications with the LINCS 2 microcomputer are activated. (At worst, main processing finishes in 19 ms, and the LINCS period fits the NTSC LINCS field period rule of 15 to 20 ms.)

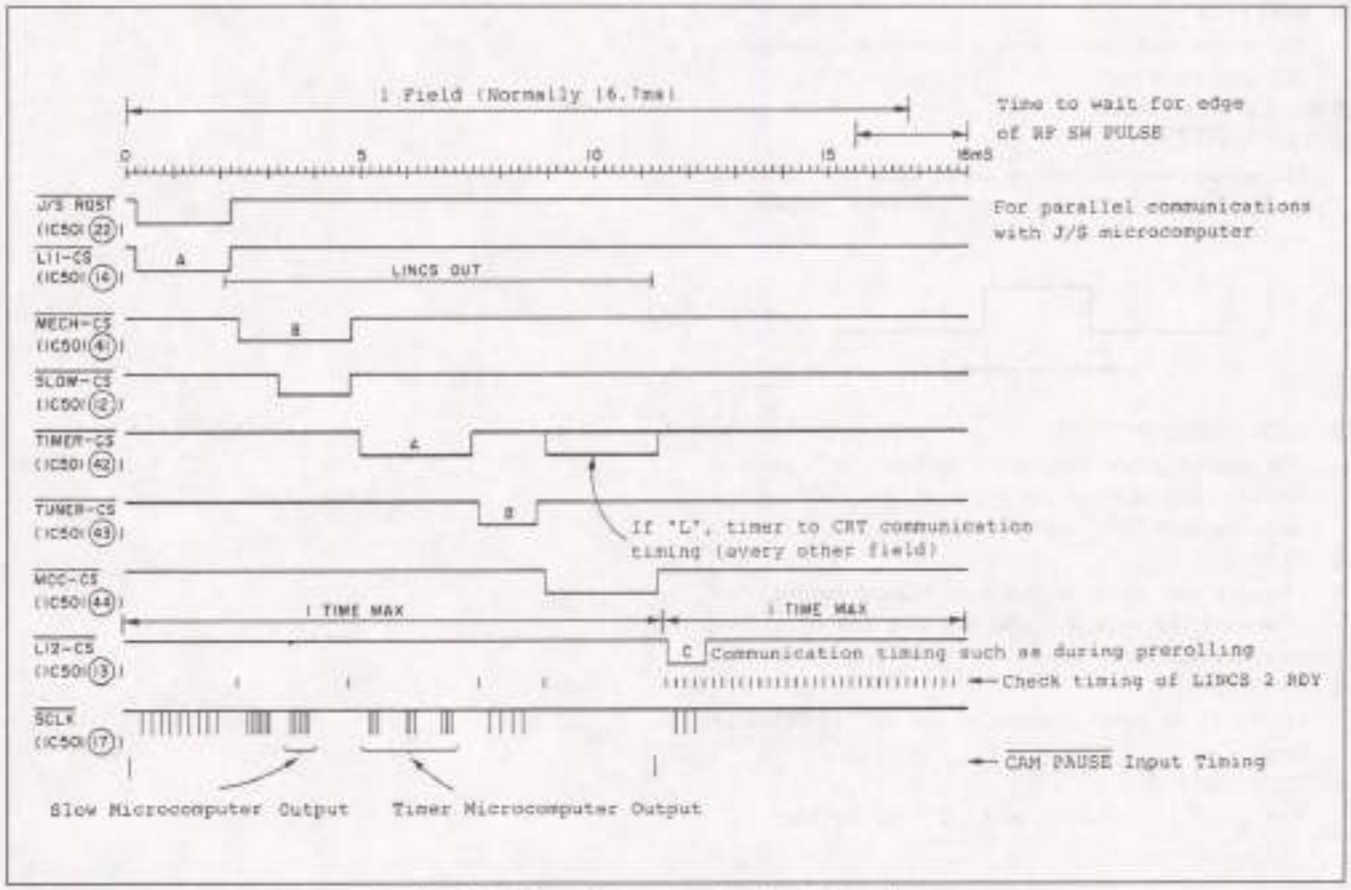


Fig. 2-2 Data bus communication timing chart

(3) Serial communications between mode controller and mechanical control and between mechanical control and slow microcomputer

1. Serial communications between mode controller and mechanical control

The mode controller and mechanical control have two-way serial communications. The mode controller outputs the serial clock (SCK). The mode controller transfers data of 48 bits making one field as a unit to the mechanical control. Six sets of data is transferred combining eight bits as one set. The first four bits are acategory code and are always the same. Data transfer from the mechanical control to the mode controller is the same. The mode controller transfers to the mechanical control such data as mode commands for mode shifting, index mode flags, data for tape balance calculation and REC BETA mode.

The mechanical control transfers to the mode controller such data as the MECHANICAL mode, index No., PB BETA mode, tape balance, CASSETTE IN and REC PROOF.

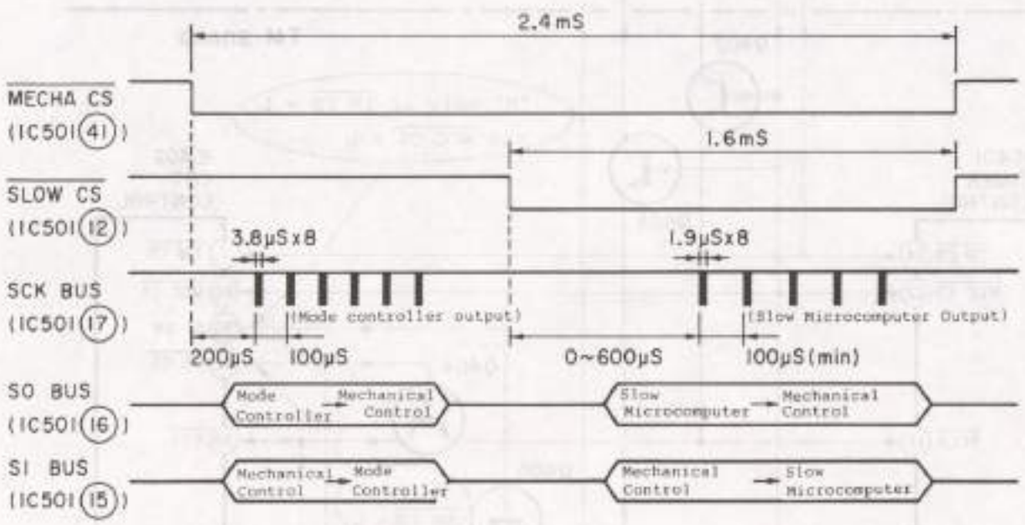


Fig. 2-5 Communication timing of mechanical control between mode controller and mechanical control between slow microcomputer

2. Serial communications between mechanical control and slow microcomputer

The mode controller holds the level of the MECH CS signal to "L" and changes that of the SLOW CS signal (Pin ⑫ of IC501) to "L" also after finishing serial communications with the mechanical control to release the communication bus line to serial communications between the mechanical control and slow microcomputer. The slow microcomputer outputs the serial clock at this time. Five sets of data combining 8 bits as one set are transferred both ways during this communication period.

The mechanical control transfers to the slow microcomputer such data as tape balance calculation data (BETA mode, TAPE SELECT, etc.), index write/erase control signals, slow control signals, and data for output to the mechanical control expansion port as the mechanical control.

The slow microcomputer transfers tape balance data to the mechanical control.

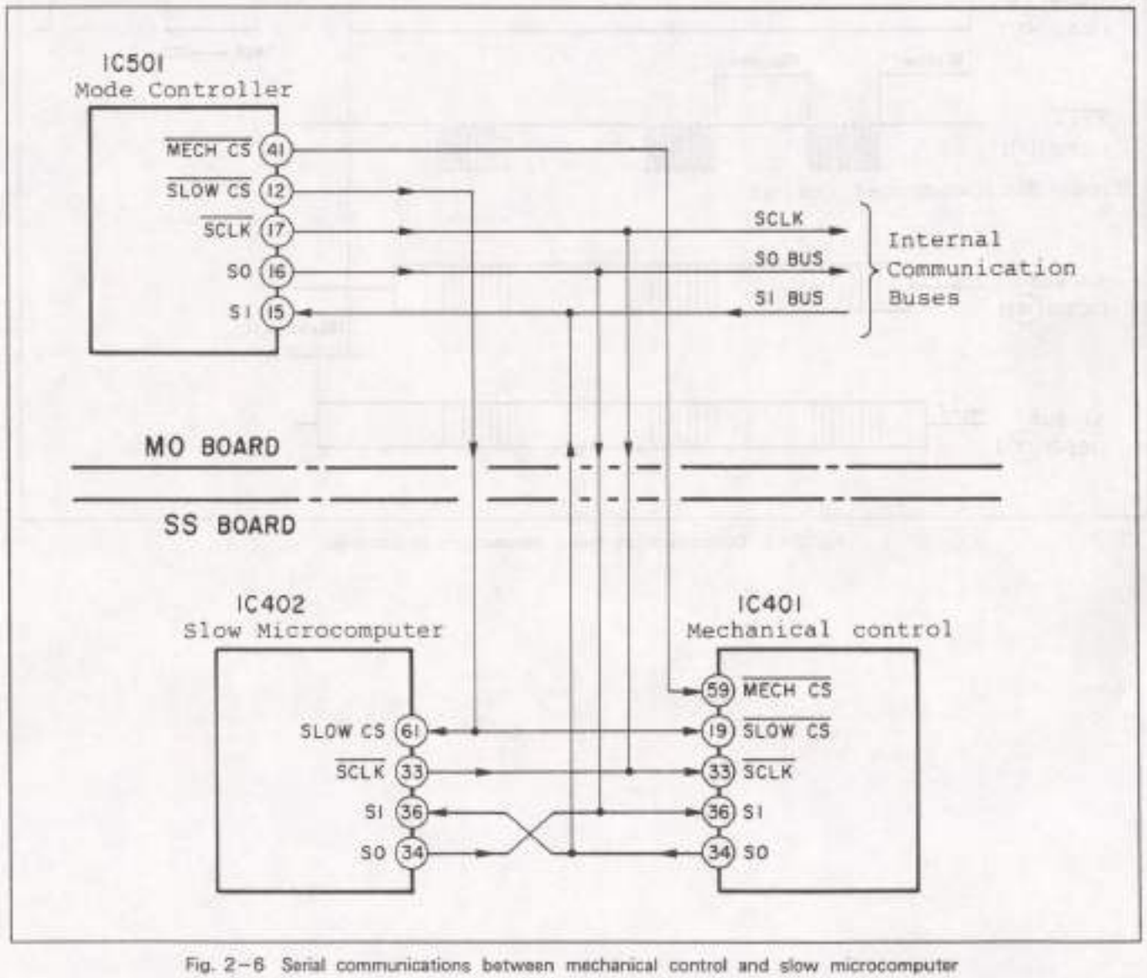


Fig. 2-6 Serial communications between mechanical control and slow microcomputer

(2) Serial communications between mode controller and timer microcomputer/CRT microcomputer.

The mode controller and timer microcomputer have two-way serial communications. The serial clock ($\overline{SCLK}$) is output by the timer microcomputer.

Data of 144 bits in units of two field is transferred from the mode controller to the timer microcomputer. Nine sets of data is transferred per field making 8 bits as one set. Field (1) and (2) are distinguished by the category code of first 4 bits. (Lap time data is transferred in field (2) once per 8 fields. The field distinction at this time is also performed by the category code of the first four bits.) Data transfer from the timer microcomputer to the mode controller is performed similarly.

Data transfered from the mode controller to the timer microcomputer is divided as follows. Data transferred from the mode controller to the timer microcomputer is fluorescent indicator tube data (mechanical mode, index mode, edit mode, tuner data, tape counter, tape balance), key ON/OFF data (INPUT SELECT, REC MODE), data from the JOG/SHUTTLE microcomputer and others.

Data transferred from the timer microcomputer to the mode controller is timer recording control signals, timer mode, input selection status, recording BETA mode control signals, tuner control signals, etc.

The CRT microcomputer monitors the transmission data from the mode controller to the timer microcomputer for use as data screen display data.

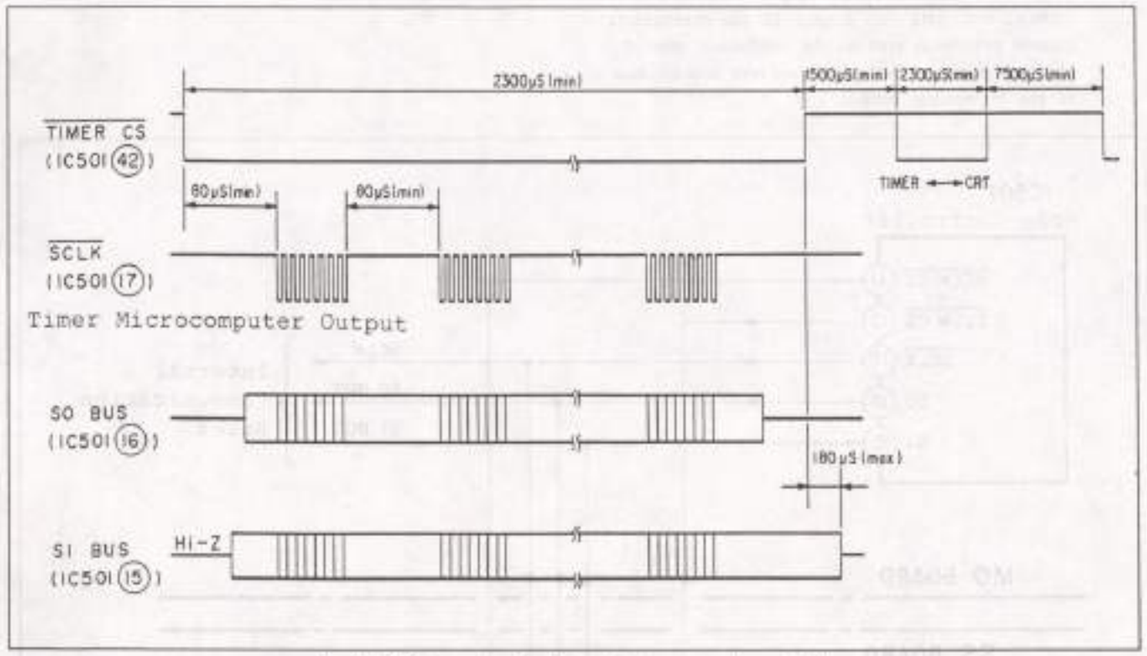


Fig. 2-3 Communication timing between mode controller

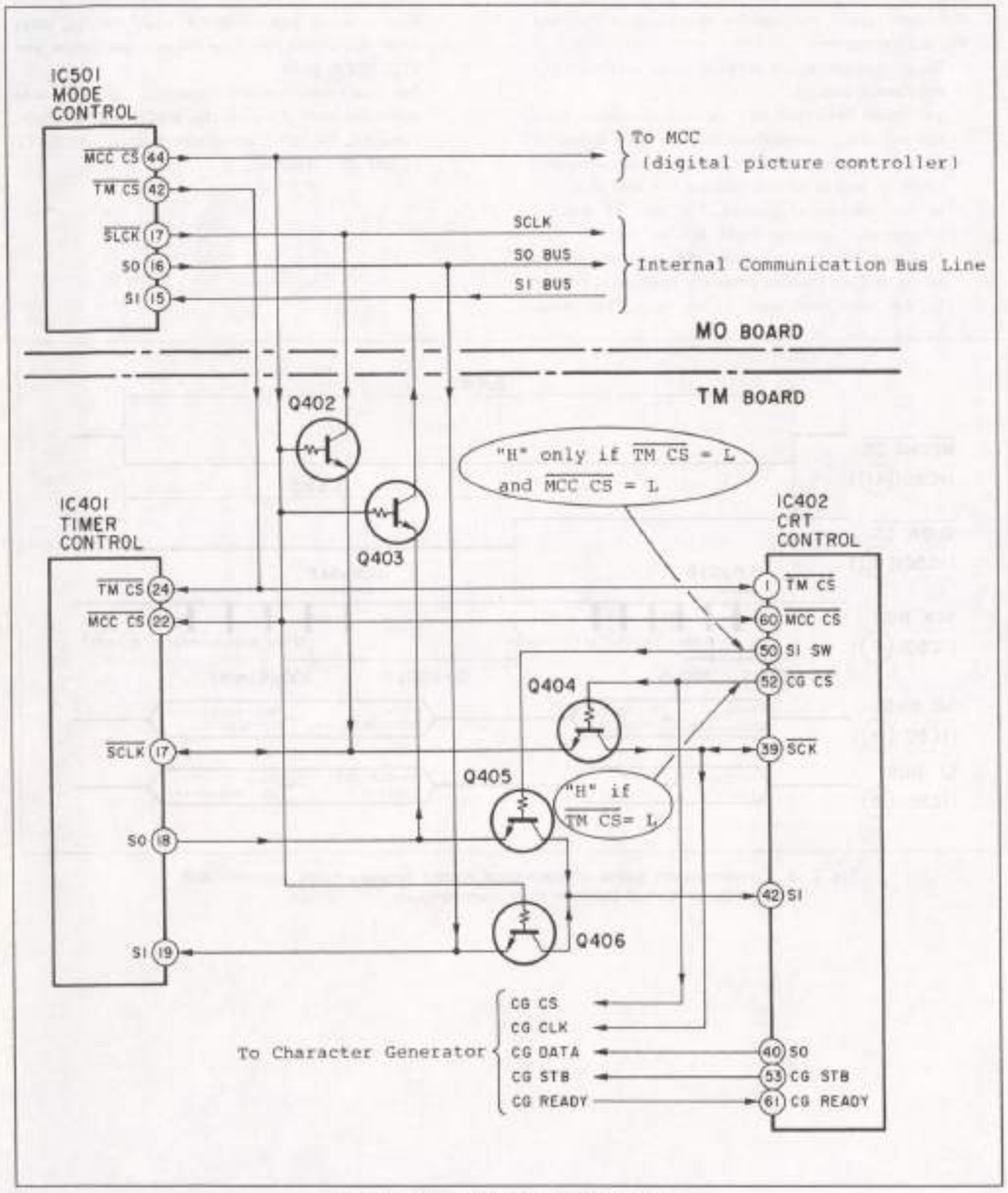


Fig. 2-4 Selection of communication buses

Data transferred from mechanical control to slow microcomputer :

- Signals output by the slow microcomputer due to shotage of mode controller ports

Signal	Slow Microcomputer Output Pin
LINE MUTE	Pin ⑥
NORM PB	Pin ①
AU EE	Pin ②
MC	Pin ③
$\overline{\text{BIAS CONT}}$	Pin ⑧
AFM REC	Pin ⑨
$\overline{\text{AFM MUTE}}$	Pin ⑩
AU INS	Pin ⑪
NOR MUTE	Pin ⑫
$\overline{\text{VD INT}}$	Pin ⑬
LIMIT S	Pin ⑭
LIMT H	Pin ⑮
UNBRK S	Pin ⑯
UNBRK H	Pin ⑰
PINCH S	Pin ⑱
PINCH H	Pin ⑲
C UNLOAD	Pin ⑳
C LOAD	Pin ㉑
C/R + ×2	Pin ㉒
REC	Pin ㉓
V MUTE	Pin ④
H SEARCH	Pin ⑤
TEN REG PL	Pin ⑫

Table 2-2

(4) Serial communications between mode controller and tuner microcomputer

The tuner microcomputer performs two-way serial communications with the timer microcomputer via the mode controller which outputs the serial clock (SCK). The mode controller (timer microcomputer) transfers to the tuner microcomputer 32 bits data making one field as one unit. Four sets of data is transferred combining 8 bits as one set. The first four bits are category code and are always the same.

The tuner microcomputer also transfers similar data tothe mode controller (timer microcomputer). The mode controller (timer microcomputer) transfers to the tuner microcomputer the tuning signal, preset mode enable signal, input select signal, power ON/OFF control signal and other information. The tuner microcomputer transfers to the mode controller (timer microcomputer) display data such as received channel and broadcasting mode (STEREO, MONO, etc.).

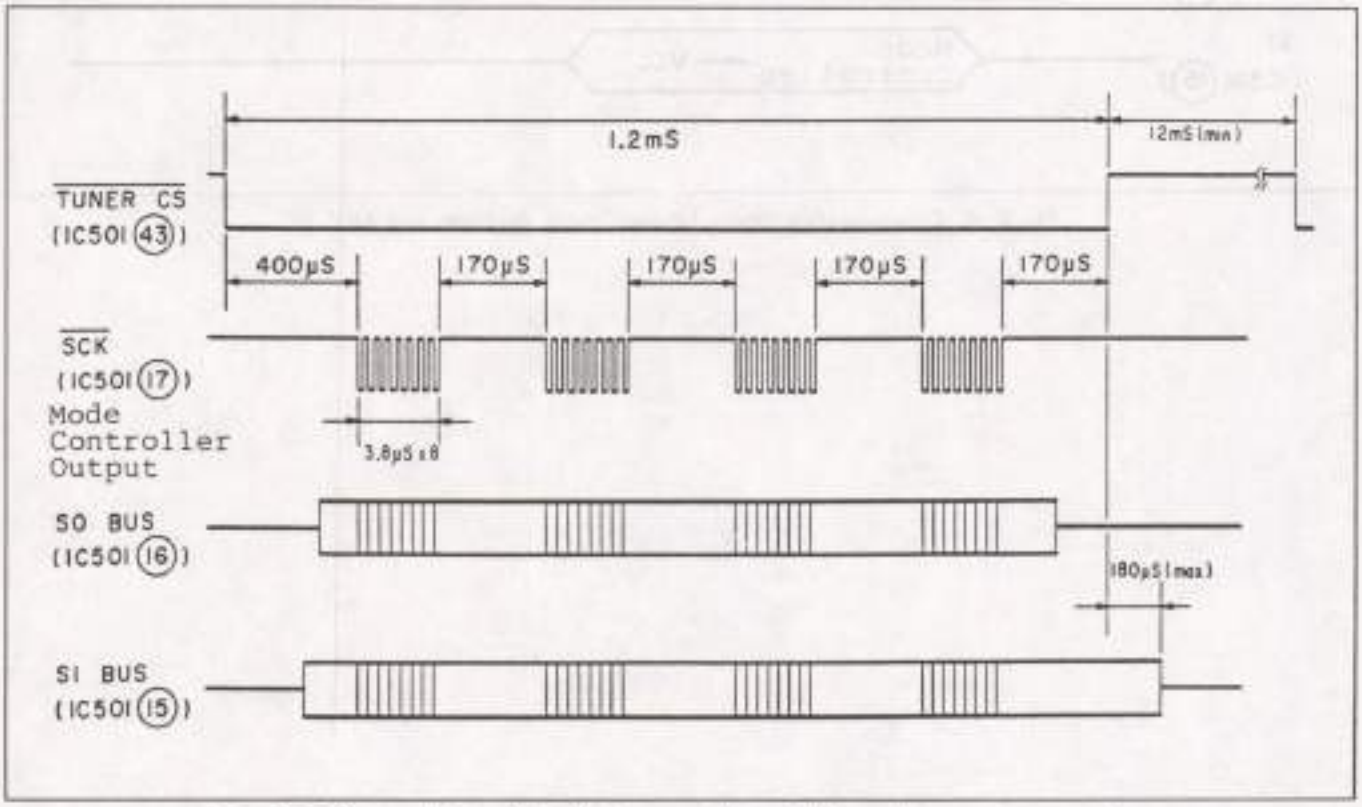


Fig. 2-7 Communication timing between mode controller and tuner microcomputer

(5) Serial communications between mode controller and MCC (digital picture controller)

The mode controller performs two-way serial communications with the MCC (digital picture controller) and outputs the serial clock (SCLK). The mode controller trnasfers data in 32 bits to the MCC making one field as one unit. Four sets of data is transferred combining 8 bits as one set. The first 4 bits are a category code and are always the same. Data transfer from the MCC to the mode controller is the same. The timer microcomputer transfers data to the CRT microcomputer while the mode controller communicates with the MCC.

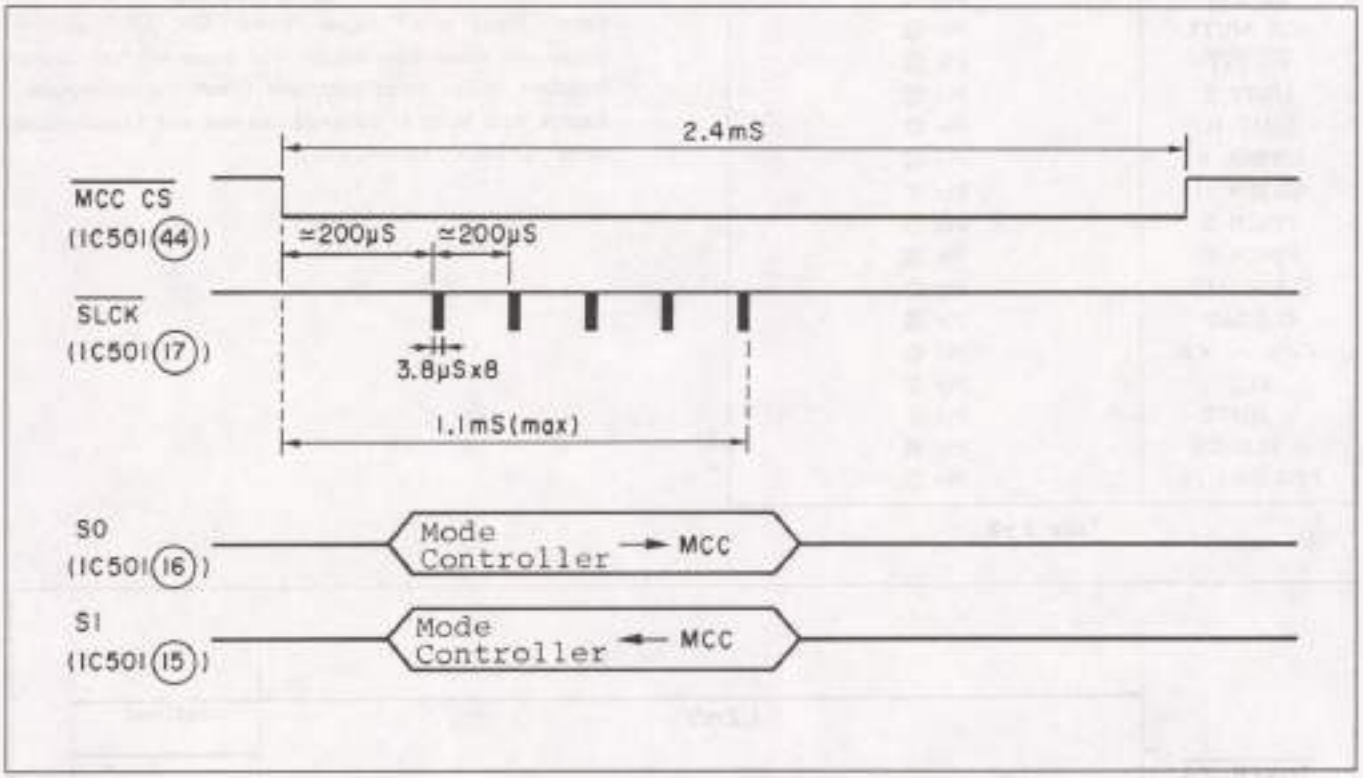


Fig. 2-8 Communication timing between mode controller and MCC

(6) Serial communications between mode controller and LINCS 2 microcomputer

The mode controller performs two-way serial communications with the LINCS 2 microcomputer and outputs the serial clock (SCK).

The LINCS 2 microcomputer transfers edit commands to the slave unit through Pin Control T. If a VTR is connected to Pin Control T, the communication period confirms to the VTR and is about period V (approx. 16.7 ms). The period is roughly 45 ms if no equipment is connected to Pin Control T.

The mode controller transfers to the LINCS 2 microcomputer data for 3 bytes (24 bits) making one communication session as one unit. Data transfer from the LINCS 2 microcomputer to the mode controller is similar. The data differs depending on whether or not a VTR is connected to Pin Control T, namely, whether to use Control T or S for connection between VTRs during editing.

When Control T is used :

The mode controller transfers to the LINCS 2 processing microcomputer control data to the LINCS 2 microcomputer (Control T/S output selection, control signal output ON/OFF and other codes) and commands to the VTR on the other side (LINCS commands). The LINCS 2 microcomputer transfers to the mode controller data whether or not Control T communications are normal and data showing the operation status of the VTR on the other side.

When Control T is used :

The mode controller transfers to the LINCS 2 microcomputer control data to the LINCS 2 microcomputer, Control S output category codes and commands. The LINCS 2 microcomputer transfers to the mode controller data showing the status of Control T communications.

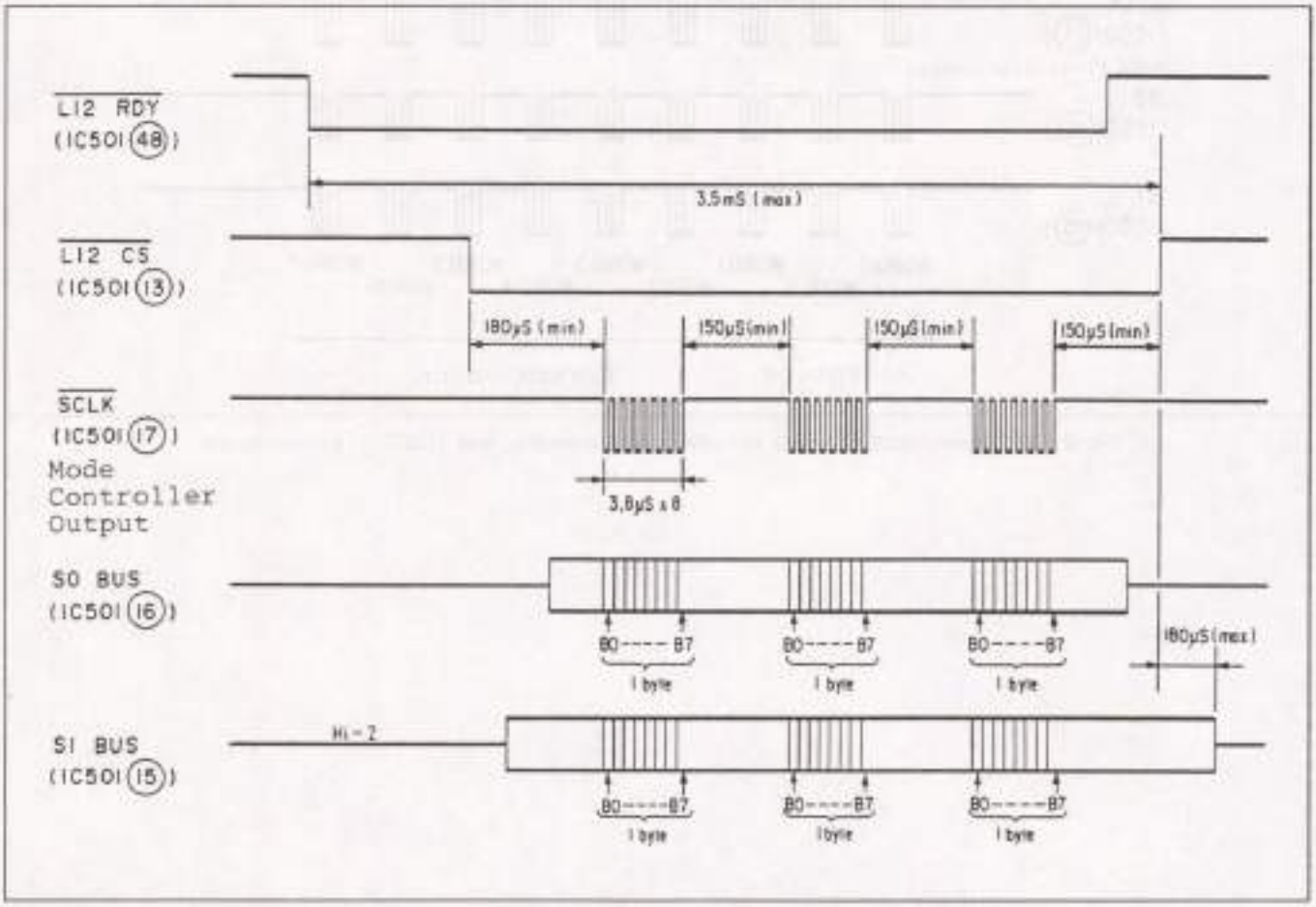


Fig. 2-9 Communication timing between mode controller and LINCS 2 microcomputer

(7) Serial communications between mode controller and LINCS 1 microcomputer

The mode controller programs two-way serial communications with the LINCS 1 microcomputer and outputs the serial clock (SCK).

The LINCS 1 microcomputer is for Control L communications and for SIRCS communications and has the same functions as those of the LINCS (Control L) microcomputer of the conventional VTR models. The mode controller transfers to the LINCS 1 microcomputer data of 9 words (8 bits per word). Six words, WORD 2 to WORD 7, are used. This data corresponds to transmission data WORD 2 to WORD 7 of Control L (or Control T) and information such as the VTR mode, status, channel and counter is transferred.

The LINCS 1 microcomputer transfers to the mode controller data of 9 words also. Only three words, WORD S to WORD 1, are actually used. WORD S transfers commands from the infrared remote commander or from Pin Control S. WORDs 0 and 1 transfer commands from Pin Control L or T.

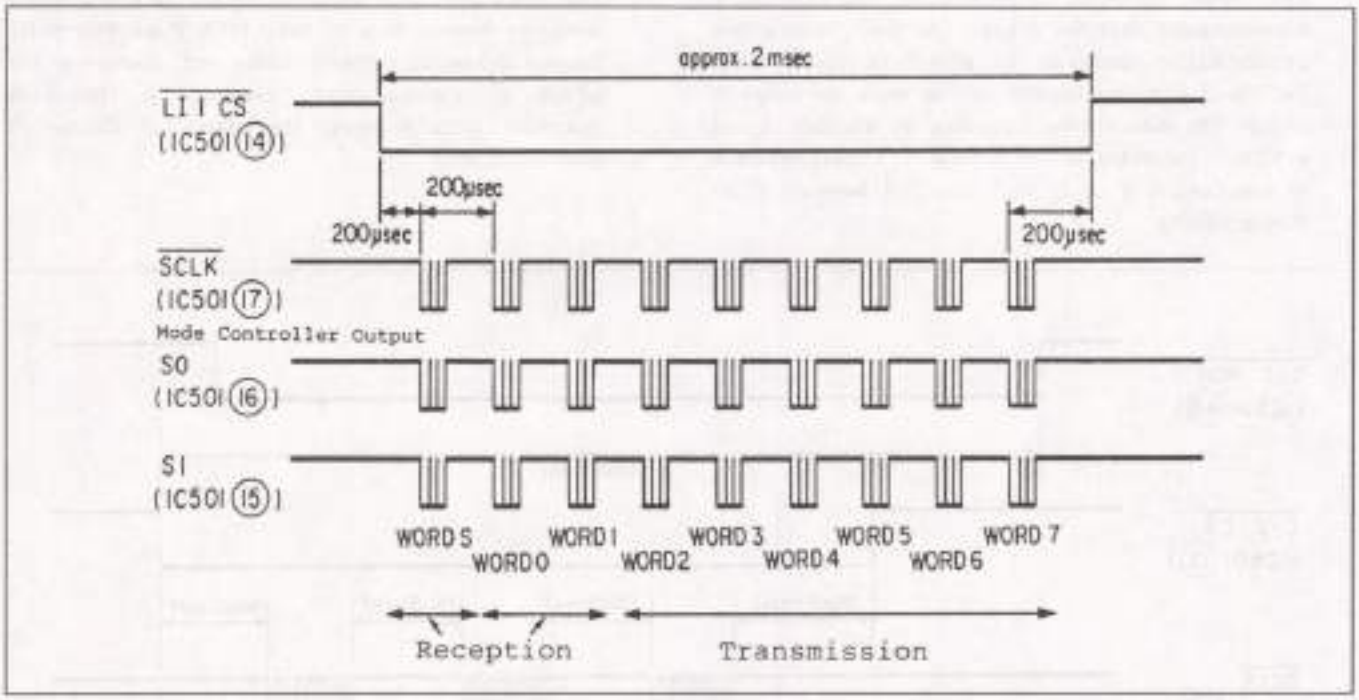


Fig. 2-10 Communication timing between mode controller and LINCS 1 microcomputer

2-1-3. Indexing Functions

The mode controller controls the mechanical control and performs indexing.

(1) Outline of functions

- Index scanning
  Continuous indexing play function of the program introductory part. The program start part is played by skipPing 10 sec each by FF or REW.
- Index search
  Program indexing play function. The start part of program before or after the present tape position by the designated number is located and is played. Addresses 1 to 19 can be designated.
- Indexing write
  The program indexing signal (INDEX-CTL) is written.
- Index erase
  The program indexing signal indexed by index scanning or index search is erased.

(2) Operation switch buttons

- Index mode selection
  INDEX : Performs INDEX SCAN/INDEX SEARCH selection and INDEX SEARCH address designation.
  MARK : Performs manual writing of index signal (INDEX CTL signal) during PB or REC.
  ERASE : Performs erasing of index signal of the program indexed by INDEX SCAN/INDEX SEARCH.
- Running direction selection
  FF : Performs INDEX SCAN/INDEX SEARCH by FF.
  REW : Performs INDEX SCAN/INDEX SEARCH by REW.

(3) Display

No. : Displays address (0 to 19) on fluorescent indicator tube (or on the monitor screen) during INDEX operation.
INDEX : Displays the INDEX operation status by combination with SCAN display.
SCAN : Displays INDEX operation status in Combination with INDEX dispaly.

2-1-4. Edit Function

(1) Assemble editing

The mode controller on the player side controls assemble editing.

1. ASSEMBLE setting

   Press the [ASSEMBLE] pushbutton switch to set up the assemble mode and to set the start and end points. By pressing the [MARK] pushbutton switch at the start or end point, the counter value at this point is stored in the internal RAM of the mode controller. The memory capacity is maximum 8 events.

2. ASSEMBLE execution

   Press the [START] pushbutton switch after finishing setting a program on the play side to start automatic ASSEMBLE editing. The descriptions below show the play side on left and recording side on right.

1. The mode controller checks that the recording side is set to the PB PAUSE mode through Control T communications.
2. Rewinds the tape to start point of event 1.
3. Returns to 6 seconds before the start point and sets to the PB PAUSE mode after sending side by Control T communications.

(The recording side should be set to the recording start point and in the PB PAUSE mode.)

4. Returns to 5 seconds before the start point on the recording side and sets to the PB PAUSE mode after receiving the "EDIT STAND BY" command.

5. Sends the "PBG" command to the recording side and enables both the recording and play sides to release pausing simultaneously after the recording side sets to the PB PAUSE mode.

6. Releases pause by the "PB" command.

7. Sends the count down commands "BEFORE IN 15", "BEFORE IN 14" and "BEFORE IN 13" to the recording side 15 fields before the start point. Shows the start point with "IN POINT".

8. Starts PB-ASSEMBLE mode shifting 8 fields before and recording with "IN POINT".

9. Sends the count down commands "BEFORE OUT 15", "BEFORE OUT 14", "BEFORE OUT 13", . . . , "OUT POINT" to the recording side 15 fields before (end point + 2 seconds).

10. Excutes mode shifting from ASSEMBLE to PB mode and sets to the PB PAUSE mode after returning to 2 seconds befoer if the OUT POINT command is sent.

11. Searches the next start point after sending "OUT POINT". Steps 2 to 9 are repeated till all the recorded events are finished.

The Control T communication path during ASSEMBLE execution is as follows :

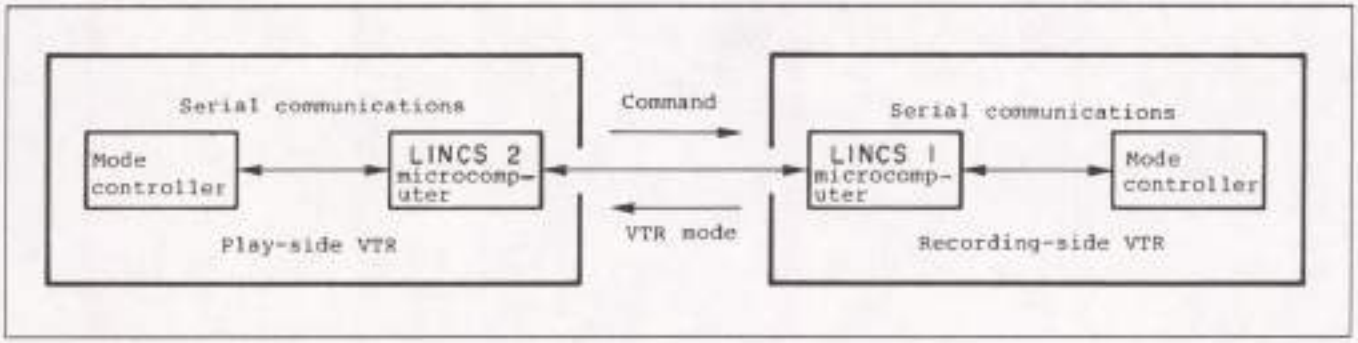


Fig. 2-11

(2) Insert editing

The mode controller on the recording side controls insert editing.

1. Insert setting

   Press the [INSERT] pushbutton switch to shift to the insert mode. Set up the PB PAUSE mode at the start point and press the [MARK] pushbutton switch to store the counter value at the start point in the internal RAM of the mode controller. The procedures are the same for the end point.

2. Insert excution

   Set the insert point on the recording side and press the [START] pushbutton switch to start automatic insert editing. The descriptions below show the play side on left and recording side of right.

(The play side should be set to the play start point and in the PB PAUSE mode.)	
	1. The mode controller checks that the play side is set to the PB PAUSE mode through Control T communications.
	2. Sends the "EDIT STAND BY" command to the play side by Control T communications and resets the recording side to 5 seconds before the start point simultaneously, setting up the PB PAUSE mode thereafter.
3. REturns to 5 seconds before the play start point and sets to the PB PAUSE mode after the recording side sends the "EDIT STAND BY" command.	
	4. Sends the "PB" command to the play side to simultaneously release PAUSE on both the recording and play sides after the play side sets to the PB PAUSE mode.
5. Release PAUSE by the "PB" command.	
	6. Starts mode shifting from PB to INSERT 8 fields before the start point and starts recording at the start point.
	7. Starts mode shifting from INSERT to PB 6 fields before the end point and ends INSERT operation at the end of point.
	8. The recording side performs PB operation for 2 seconds from the end point and sends the "PAUSE" command to the play side. The recording side returns to the end point and sets to the PB PAUSE mode.
9. Releases PAUSE by the "PAUSE" command.	

The Control T communication path during INSERT execution is as follows:

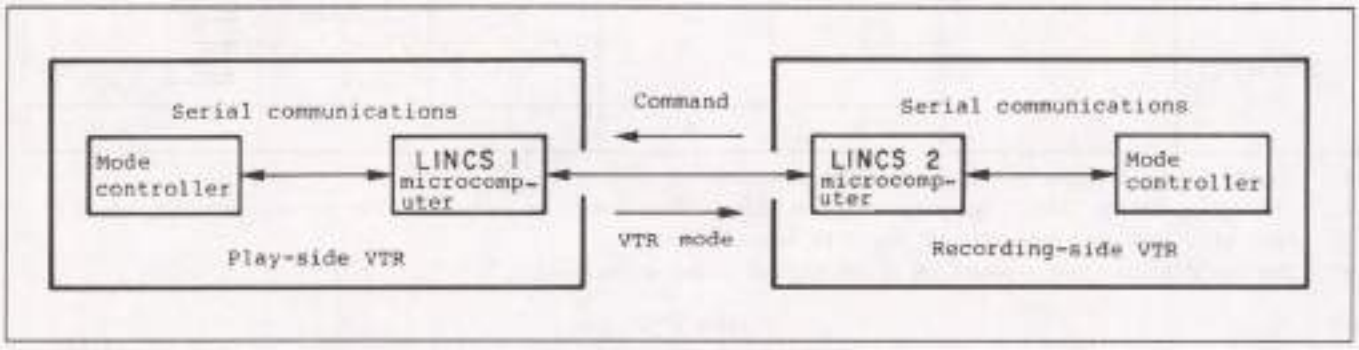


Fig. 2-12

(3) Compacted editing

Operation of pushing the START pushbutton switch without setting the editing points (start and end points) after setting up the ASSEMBLE edit mode is regarded as COMPACTED editing. Editing starts making the tape position in which the START pushbutton switch is pressed as the start point. In COMPACTED editing, all the set points are cleared when editing ends (ended by pressing the PAUSE or STOP pushbutton switch), returning to the start point of PROG 1 (event 1) to wait for input.

This function enables high-precision editing with minimal operation by repeating start point search, pressing START pushbutton switch, pressing PAUSE pushbutton switch at end point.

2-1-5. Audio Monitor L/R Selection

The functions of the AUDIO MONITOR L/R pushbutton switch differ in accordance with the three conditions-VTR mode, INPUT SELECT mode and $\overline{\text{MONI IND}}$ signal ("L" during BETA HIFI play). The tuner microcomputer selects AUDIO MONITOR MAIN/SUB by communication with the mode controller. The audio control signals are $\overline{\text{R CONT}}$ and L CONT.

2-2. MECHANICAL CONTROL (MECH CON) MICROCOMPUTER

The work of the MECH CON microcomputer is principally as follows.

- Mechanical mode control (MODE CON)
  Excutes mode transition of the mechanism, servo, video, audio, and digital picture circuits by "mode commands" sent by serial communications from the MODE CON.
- Index control
  Excutes index search and index scan operations by index mode flags sent from the MODE CON by serial communication. Detailed control during index write and erase is carried out by the SLOW microcomputer (IC402).

VTR mode	INPUT SELECT mode Operation Switch Block (A) S005		$\overline{\text{MON IND}}$ IC501 ⑮ MO-5 Board	$\overline{\text{L-CONT}}$ IC502 ⑱ TU-86 Board	$\overline{\text{R-CONT}}$ IC502 ⑲ TU-86 Board	Fluorescent Indicator Tube Display	AUDIO MONITOR MAIN/SUB Selection Operation Switch Block (A) S003
REC EE V INSERT AV INSERT Includes EE mode by EE pushbutton switch.	TUNER	STEREO *1	L	L	L	STEREO	
		MONO *1	L	L	L		
	SIMUL		L	L	L	STEREO	
	LINE		L	L	L	STEREO	
			H	L	L		
A INSERT			L	L H L	L L H	STEREO L R	
			H	L	L		

*1 Change by the mode of received broadcast program.

*2 The during PB/A INSERT selection enable is stored unless power is turned off. The previous status resets if reset after shifting temporarily to oter VTR mode.

*3 The initial status during power on is the highest status of each mode.

Table 2-3

2-2-1. Mechanical Control Microcomputer Terminal Functions

Terminal No.	Port	Signal	I/O	Function
1	PB1	INDEX WRITE	O	Index write signal. Normally "L". "H" during index write or erase.
2	PB2	$\overline{C/R}$ (C)	O	CUE/REVIEW signal for servo circuit. "L" when CUE/REVIEW.
3	PB3	×2	O	Double speed signal. "H" when double speed playback.
4	PE0	PB TRACON	O	Tracking control REC/PB switching signal. "L" when in REC, REC PAUSE, FF, REW, STOP or DIGITAL SCAN mode.
5	PE1	CAP STOP	O	Capstan motor ON/OFF signal. "L" when capstan motor is operating.
6	PE2	DRUM STOP	O	Drum motor ON/OFF signal. "L" when the drum motor is operating.
7	PE3	REC • P	O	REC signal for servo circuit. H" when REC.
8	PF0	TAPE SPEED A	O	Capstan speed switching signal.
9	PF1	TAPE SPEED B	O	
10	PF2	TAPE SPEED C	O	
11	PF3	$\overline{FG\ MASK}$	O	CAPSTAN FG masking signal. Masking when "L". Momentarily "L" during ×2 → PB, CUE → PB or REV → −1 mode transition.
12	PC0	FR ON	O	Framing servo ON/OFF signal.
13	PC2	βIII NP	O	"H" only when in the βIII REC, PB, ×1, INSERT, ASSEM, or CUE mode.
14	PC2	βII NP	O	"H" only when in the, βII REC, PB, ×1, INSERT, ASSEM, or CUE mode.
15	PC3	AFC INH	O	"H" in the REC, REC PAUSE, INSERT (V or AV) and INSERT PAUSE (V or AV) mode.

Mode	β Mode	Tape Speed A (8)	Tape Speed B (9)	Tape Speed C (10)
×1, INS, ASSEM ×1 REC, PB	I II III	H L L	L H H	L L H
×2 −×2	I II III	H H L	L L L	L L H
CUE	I II III	H L L	H L L	H L H
REV	I II III	H L L	H H L	H L H
PAUSE FRAME FEED SLOW	I II III	H L L	L H H	L L H
STOP, LOADING FF, REW		× ×	× ×	× ×

Table 2-4 (1)

Terminal No.	Port	Signal	I/O	Function
16	PD0	$\overline{\text{CAP LOCK}}$	I	Capstan servo phase lock detecting signal. "L" when the capstan servo becomes stable.
17	PD1	$\overline{\text{DRUM LOCK}}$	I	Drum servo phase lock detecting signal. "L" when the drum servo becomes stable.
18	PD2	$\overline{\text{SKEW IN}}$	I	Not used.
19	PD3	$\overline{\text{SLOW CS}}$	I	Communications between MECH control and SLOW microcomputer when the MECH CS signal and this CHIP SELECT signal are "L".
20	PG0	REEL FWD	O	Reel motor circuit direction control signal. "L" when rotating in reverse.
21	PG1	REEL STOP	O	Reel motor ON/OFF signal. "L" when the reel motor is operating.
22	PG2	FF/REW (R)	O	FF/REW signal for the reel motor control circuit (IC501). "H" when FF/REW.
23	PG3	REEL LOW	O	Reel motor control signal. "L" when reel motor is operating at high speed (during FF/REW).
24	PH0	$\overline{\text{C/R}}$ (R)	O	CUE/REVIEW signal for the reel motor control circuit (IC501). "L" during picture search or FR search.
27	PH1	CAP FWD	O	Capstan motor circuit direction switching signal. "H" when a forward direction circuit.
28	PH2	SLOW	O	"H" when slow playback, frame feed or pause.
29	PH3	STEP	O	Control signal to the SLOW microcomputer. "H" pulse during SLOW control.
30	XTAL			Terminal for clock oscillation Clock frequency 4.19 MHz.
31	EXTAL			
32	$\overline{\text{RST}}$	$\overline{\text{RESET}}$	I	Initial reset signal from the timer microcomputer (IC401 of board TM-92). "L" when reset.
33	PX0/SC	SCK BUS	O	• Serial communications clock input terminal • Serial communications data output terminal • Serial communications data input terminal Conduct serial communications between the mode control (IC501 of Board MO-5) and SLOW microcomputer (IC402).
34	PX1/SOB	SO (SI BUS)	O	
36	PX3/SI	SI (SO BUS)	I	
35	PX2/SOA	C DOWN SW	I	"L" when the cassette compartment is lowered.
37	PY0	T UNLOAD	O	Threading motor control signal. "H" during tape unthreading operation.
38	PY1/$\overline{\text{PWM}}$	T LOAD	O	Threading motor control signal. "H" when threading tape.
39	PY2/WP	β MODE A	I	Input of BETA mode discrimination results of the playback tape. Discrimination of BETA mode is carried out in the JOG/SHUTTLE microcomputer (IC502 of the MO-5 board).
40	PY3/$\overline{\text{EC}}$	β MODE B	I	

BETA mode of the playback tape	β Mode A	β Mode B
β I	L	L
β II	H	L
β III	L	H

Table 2-4 (2)

Tarminal No.	Port	Signal	I/O	Function
41	PL0	V PB	O	"H" when the video circuit (VI board) is set to playback state.
42	PL1	V REC	O	"H" when the REC/PB amp (RP board) is set to record state.
43	PL2	PRE REC	O	"H" when the power supply of the recording head amp (RP board) is set to ON.
44	PL3	OVER REC	O	"L" during the period that there is no overwrite in the REC, INSERT (AV/V) or ASSEMBLE mode. This signal increases the recording current during the overwrite period.
46	PK0	REEL FG (S)	I	FG signal input of the supply side reel. Pulse input of frequencies proportional to reel rotation. This is used to detect abnormalities in the drive system.
47	PK1	REEL FG (T)	I	FG signal input of the takeup reel side. Pulse input of frequencies proportional to reel rotation. This is used to detect abnormalities in the drive system.
48	PK2/T1	RF SW P	I	RF SW PULSE input.
49	PK3/PMI	VD/CTL	I	VD (REC CTL) signals are input during REC and CTL (PB CTL) signals are input during PB.
50	PI0	V EE	O	EE signal for the video circuit. "L" when the video circuit is in PB state. Becomes "H" even in the PB mode if the EE button is pressed.
52	PI2	$\overline{\text{B FE}}$	O	"L" when the B CH flying erase head is operating.
53	PI3	$\overline{\text{A FE}}$	O	"L" when the A CH flying erase head is operating.
54	PJ0	CKG SW	I	"L" when the conventional Beta cassette is inserted.
55	PJ1	CKG REC PROOF	I	"H" when the ED Beta cassette is in erasure prevention state.
56	PJ2	MECHA SW	I	THREADING END SW input. "L" when threading is in completed state.
57	PJ3	INDEX DET	I	Input of INDEX DET circuit (IC010) output signal. "H" during INDEX detection.
59	INT	$\overline{\text{MECH CS}}$	I	CHIP SELECT signal from MODE control to MECH control.
60	PA0	REC PROOF	I	REC PROOF SW input for the conventional Beta cassette. This switch also serves as the CASSETTE IN switch. "H" when the erasure prevention tongue of the cassette is broken off or when the ED Beta cassette is inserted.
61	PA1	$\overline{\text{TAPE END}}$	I	Input of the TAPE END detecting circuit (IC403) output signal. "L" at tape end or tape top.
62	PA2	TOP/$\overline{\text{END}}$	O	Tape top/tape end detection switching signal. "L" when tape end detected (forward feed).
63	PA3	RESET 194	O	Reset signal for the digital servo IC (IC006). 50 msec "H" pulse when servo operation starts.
64	PB0	CTL GAIN	O	Gain switching signal of the PB CTL amp. "H" during high speed travel (FF, REW, CUE, REV, DIGITAL SCAN).

Table 2-4 (3)

2-2-2. Mode Transition Timing Chart

Mode control of the mechanism section, system control peripheral circuits, servo circuit, video circuit, and audio circuit is carried out by MECH control. The timing chart of the principal mode transitions follow. To explain interpretation of the timing chart, transitions of the STOP → PB, STOP → REC modes and the cassette loading, tape threading and eject (tape unthreading, cassette unloading) operations will now be described.

STOP → PB

1. The following operations are executed first.
   - Resets servo IC (IC006) by setting the RESET 194 signal to "H" for a 50 msec period or rotates the drum motor by setting the DRUM STOP signal to "L".
   - Mutes the audio output by setting the LINE MUTE signal to "H".
2. The following operation is carried out 50 msec after the above.
   - Sets the CAP STOP signal to "L" and starts the capstan motor.
   - Sets the V PB signal to "L" and starts the capstan motor.
   - Sets the V PB signal to "H" and puts the video circuit (VI board) and BETA HIFI audio circuit (AU board) in playback state. Mutes the video output by setting the v MUTE signal to "H".
   - Sets the PB TRACON signal to "H" and puts the tracking control circuit in PB state.
3. Sets the REEL FWD signal and REEL STOP "signal to L" for 100 msec and separates the pendulum arm the T reel 300 msec after "2".
4. Sets UNBRK PL S signal and UNBRK PL H signal "H" and releases the brake by activating the brake solenoid 700 msec after "2".
5. Performs the following 200 msec after "4".
   - Sets the UNBRK PL S signal to "L" and puts the brake solenoid in HOLD state.
   - Sets the NORM PB signal to "H" for normal audio circuit (VE board) state.
   - Sets PINCH PL S and PINCH PL H signals to "H" and activates the oinch solenoid to press the Pinch roller against the capstan.
   - Sets $\overline{\text{VD INT}}$ signal to "L" and uses the servo reference signal as the internal reference signal (Signal obtained by frequency division of the 3.58 MHz signal in the servo IC).
6. Carries out the following operation 400 msec after "4".
   - Returns the PINCH PL S signal to "L" and puts the Pinch solenoid in HOLD state.
   - REEL STOP signal is set to "L" with the REEL FWD signal set to "H". This causes the reel motor to turn forward, the pendulum arm to return to the T reel side and the T reel to start tape takeup.
7. V MUTE signal is set to "L" 2100 msec after "4" andvideo output mute cleared.
8. The following operation is carried out 100 msec after "7".
   - Clears Beta HIFI audio output mute by setting the $\overline{\text{AFM MUTE}}$ signal to "H".
   - Clears audio output mute by setting the LINE MUTE signal to "L".

STOP → REC

This mode transition is divided into the STOP → REC PAUSE and the REC PAUSE → STOP mode transitions.

<STOP → REC PAUSE>

1. Executes the following operation first.
   - Resets the servo IC by setting RESET 194 signal to "H" for 50 msec and also starts the drum motor by setting the DRUM STOP signal to "L".
2. Performs the following operation 50 msec after "1".
   - Sets REEL FWD signal to "L" and reverses the reel motor. The FF/REW (R) signal is set to "H" and the reel motor drive voltage raised about 4 Vdc. (Reel still does not turn.)
   - Sets CAP FWD signal to "L" and reverses the capstan motor. (Capstan motor still does not start.)
   - Sets the TOP/END signal to "H" and operates the tape top sensor.
   - Sets the REC signal to "H" and notifies the CAMERA MODE circuit of the transition to REC state.
3. Performs the following operation 400 msec after "2".
   - Sets the REEL STOP signal to "L" for a period of 100 msec and swings the pendulum arm to the S reel side.
   - Sets the UNBRK PL H signal to "H" and releases the brake by activating the brake solenoid.
4. Performs the following operation 600 msec after "2".
   - Returns the UNBRK PL S signal to "L" and puts the brake solenoid in HOLD state.
   - Sets the PINCH PL S signal and PINCH PL "H" and presses the pinch roller against the capstan by activating the pinch solenoid.
5. Sets REEL STOP signal to "L" 700 msec after "2" and takes up the tape by rotating the T reel. The reel motor drive voltage is about 4 Vdc.
6. Performs the following operation 800 msec after "2".
   - Starts the capstan motor by setting the CAP STOP signal to "L". Since the CAP FWD signal is "L" at this time, the capstan turns in reverse and the tape is taken up on the S reel at single speed.
   - Returns the PINCH PL S signal to "L" and puts the pinch solenoid in HOLD state.
7. Counts falling of the VD/CTL signal from 1000 msec after "2".
8. When the counted value reaches 21, the SLOW signal is set "H" for SLOW control by synchronizing with the initial rise of the RF SW pulse. (If the CTL signal is not reproduced because of an unrecorded tape, operation along the dotted line of the timing chart will be carried out by setting a time limit of 1500 msec.)

9. Sets STEP signal to "H" in synchronism with the second rise of the RF SW pulse.
   Since the CAP FWD signal is "L", the SLOW signal "H" and the STILL signal (MECH CON → SLOW microcomputer communication data) is "L" at this time, the SLOW microcomputer controls SLOW of (−×1 − STILL) and stops the tape. (For details, see the SLOW microcomputer "−×1 − STILL" Timing Chart.)
10. Synchronizes with the third fall of the RF SW pulse and performs the following operation.
    - Sets TOP/$\overline{\text{END}}$ signal to "L" and operates the TOP END sensor.
    - Sets the STEP signal to "L".
    - Sets the communications data STILL to the SLOW microcomputer to "H".
11. Performs the following operation 300 msec after "10".
    - Sets the REEL FWD signal to "H" and turns the reel forward. This cause the pendulum arm to swing to the T reel side. At the same time, the FF/REW (R) signal becomes "L" so the reel motor drive voltage subsequently becomes about 2.7 Vdc.
    - Sets CAP FWD signal and CAP STOP signal " to H". This causes the capstan motor to stop and the direction of turn of the capstan motor will subsequently be in the forward direction.
12. Sets the REEL STOP signal to "H" 500 msec after "10" and stops the reel motor.
    The foregoing completes the STOP − REC PAUSE mode transition.

<REC PAUSE → REC>

13. Performs the following operation immediately after the STOP → REC PAUSE mode transition is completed.
    - Sets the REEL STOP signal to "L". This causes the reel motor to turn forward and the T reel to start taking up the tape.
    - Sets CAP STOP signal to "L".
    - Sets the FR ON signal to "L" and turns framing servo OFF.
14. Synchronizes with the RF SW pulse start up and sets SLOW signal to "L" and STEP signal to "H" 50 msec after "13". Since the CAP FWD signal and the STILL signal (MECH CON → SLOW microcomputer communication data) are "H" at this time, the SLOW microcomputer performs SLOW control (STILL → PB) and causes tape speed to rise sharply.
    the STEP signal becomes "L" in synchronism with falling of the second RF SW pulse. It also starts count of falling of the VD/CTL signal.
15. When the counted value reaches 12, it sets the $\overline{\text{BIAS}}$ $\overline{\text{CONT}}$ signal to "L" and operates the full head. Recording of the normal audio signal also starts st this time.
16. Performs the following operation during fall of the initial RF SW pulse (In the BERA Ⅱ mode) after the counted value reaches 14.
    - Sets the PRE REC signal to "H" and puts the head amp (RP board) in recording state.
    - Sets the $\overline{\text{B FE}}$ signal to "L" and operates the B CH flying erase head.
    - Sets the AFM REC signal to "H" puts the BETA HIFI circuit in recording state.
17. Sets the V REC signal to "H", the REC/PB amp (RP board) to recording state and starts recording of the video signal and BETA HIFI audio signal during startup of the second RF SW pulse. (BETA Ⅱ mode.)
18. Sets the REC $\overline{\text{PAUSE}}$ signal to "H" at startup of the third RF SW pulse. This causes the servo circuit to be in recording state and CTL signal recording to start. (BETA Ⅱ mode.)
19. Enters the erasing area of the full erase head 12 seconds after "14". Since there is no need to operate the flying erase head, operation is stopped by setting the $\overline{\text{A FE}}$ and $\overline{\text{B FE}}$ signal to "H".

Cassette Loading and Tape Threading

1. When a cassette is inserted in the VTR, the REC PROOF SW (S951-2) is ON, and the REC PRF SW signal level (Pin ㊱ of IC401) rises, the MECH CON sets the C LOAD signal to "H" and loads the cassette by turning the cassette loading motor in the loading direction. The REC PROOF SW subsequently of the erasure prevention tongue in conventional Beta cassettes.
2. MECH CON performs the following operations when the cassette compartment descends, the CASSETTE DOWN switch (S951-1) goes ON, and the C DOWN SW signal (Pin ㉟ of IC401) becomes "L".
   1) The limiter solenoid is activated by the LIM PL S and LIM PL H signals to remove tape slack and put the reels in direct state.
   2) The reel motor control signal is set as follows to reverse the reel motor with high torque to remove tape slack on the reel side. (200 msec.)
      REEl FWD ····· "L"
      REEL STOP ····· "L"
      FF/REW (R) ····· "H"
      REEL LOW ····· "L"
3. The LIM PL Hsignal and S LOAD signal are returned to "L" 700 msec after "2" and ends cassette loading and removal of tape slack.
4. The T LOAD signal is set to "H" 1000 msec after "2" and starts tape threading by turning the tape threading motor in the forward direction. The reel motor is turned in the forward direction with a weak torque by the control signal at this time as follows.
      REEl FWD ····· "H"
      REEL STOP ····· "L"
      FF/REW (R) ····· "L"
      REEL LOW ····· "H"
5. When the threading ring turns, the LOADING END SW (S952) goes ON, and the L END SW signal (Pin ㉞ of IC401) becomes "L", the MECH CON drives the

threading motor 8 pulses by means of the T LOAD signal to ensure positive threading after stopping the threading motor by setting the T LOAD signal and T UNLOAD signal to "H".

6. After pulse drive ends, the reel brake is released by the UNBRK PL S signal and the UNBRK PL H signal. Tape slack is removed by turning the reel with a strong torque as follows by means of the reel motor control signal.
7. Stops the reel motor, operates the reel brake and ends tape threading operation.

Eject Operation (Tape Unthreading, Cassette Unloading)

REEl FWD ····· "H"
REEL STOP ····· "L"
FF/REW (R) ····· "H"
REEL LOW ····· "H"

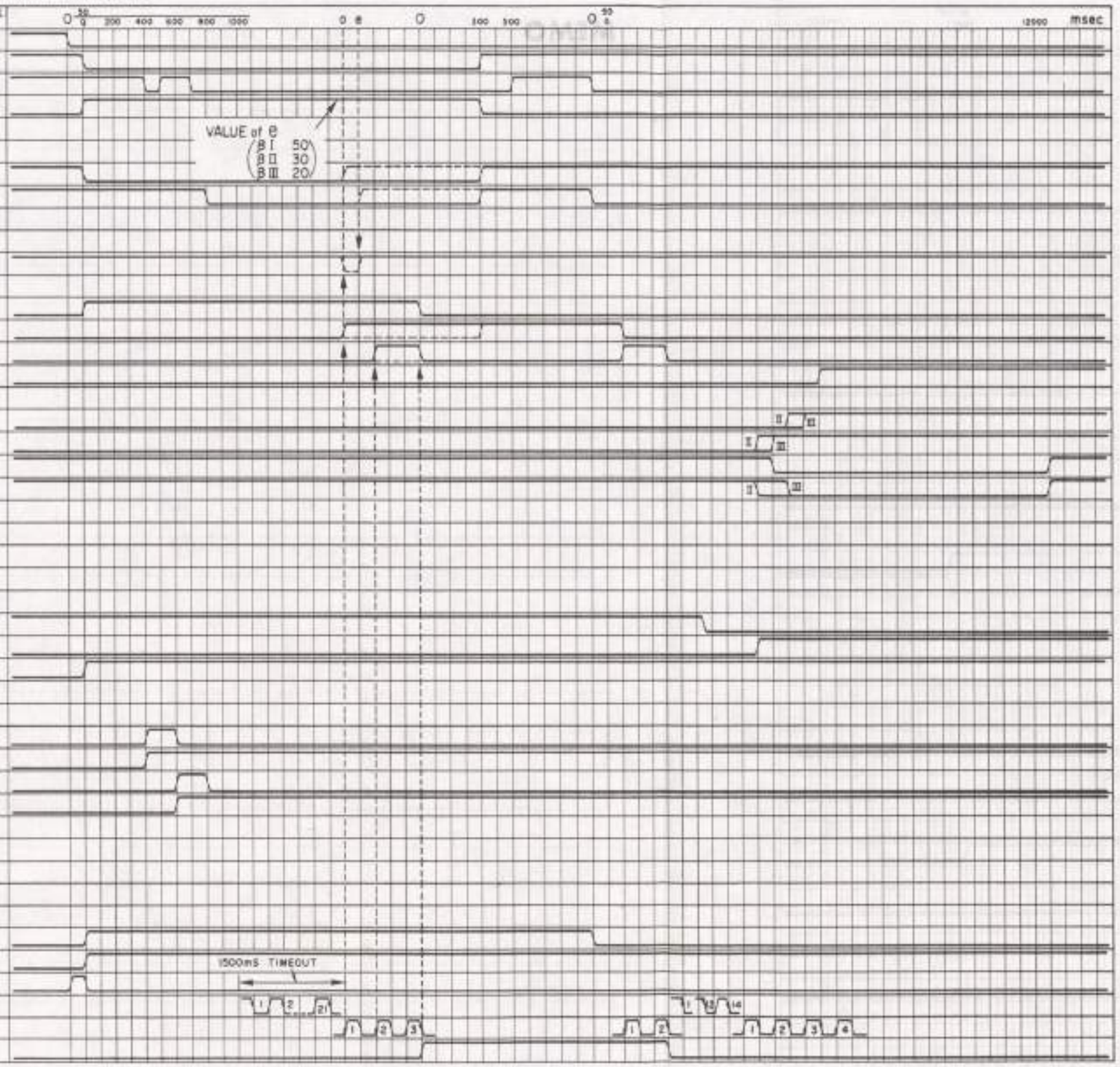
1. When the EJECT button is pressed, MECH CON first sets the TOP/END signal to "H" and operates the tape top sensor. The tape top sensor functions as the unthreading end sensor.
2. The reel brake is released by the UNBRK PL S signal and UNBRK PL H signal 50 msec after "1". The reel motor is then turned forward and the tape taken up on the T reel by setting the reel motor control signal as follows.
   Avoid reaching the top of the tape during the unthreading operation. (To use the tape top sensor as the unthreading end sensor.)

   REEl FWD ····· "H"
   REEL STOP ····· "L"
   FF/REW (R) ····· "H"
   REEL LOW ····· "H"
   C/R (R) ····· "L"
3. Returns the UNBRK PL H signal to "L" and activates the reel brake.
4. REverses the reel motor and sets to tape takeup state on the S reel side.
5. Turns the threading motor by setting the T UNLOAD signal to "H" and turns the threading ring in the unthreading direction. The reel motor control signal is set as follows at this time and the reel motor is turned in reverse to take up tape slack on the S reel. The reel motor is driven with constant since the T UNLOAD signal is "H".

   REEl FWD ····· "L"
   REEL STOP ····· "L"
   FF/REW (R) ····· "L"
   REEL LOW ····· "H"
   C/R (R) ····· "L"
6. When the threading end position is reached during threading, the tape end sensor operates and the $\overline{\text{TAPE END}}$ signal (Pin ㊾ of IC401) becomes "L". MECH CON then sets the T LOAD signal to "H" and brakes and stops the threading motor. The T load and T UNLOARD signals are then returned to "L".
7. The REEL STOP and REEL FWDsignals are set to "H" and the reel motor stopped 200 msec after "6".
8. The C UNLOAD signal is set to "H" 450 msec after "6" and cassette unloading is started by turning the cassette loading motor in the unloading direction.
9. 650 msec after "6", MECH CON monitors the REC PRF SW signal (Pin ㊽ of IC401) to detect end of ejection with the REC PROOF SW (S951-2).
10. When the cassette compartment rises and the eject operation (cassette unloading operation) ends, the REC PROOF SW is turned OFF and the REC PRF signal becomes "H", MECH CON then sets the C UNLOAD signal to "L" and stops the cassette loading motor.

2. STOP → REC Mode Transition Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	
20	REEL FWD	
21	REEL STOP	
22	FF/REW(R)	
23	REEL LOW	H
24	C/R(R)	L
27	CAP FWD	
5	CAP STOP	
2	$\overline{\text{C/R(C)}}$	H
3	x2	L
11	$\overline{\text{FG MASK}}$	
64	CTL GAIN	L
62	TOP/$\overline{\text{END}}$	
28	SLOW	
29	STEP	
7	REC $\overline{\text{P}}$	L
41	V PB	L
42	V REC	L
43	PRE REC	L
53	$\overline{\Delta\ \text{FE}}$	H
52	$\overline{\theta\ \text{FE}}$	H
* 1	NORM PB	L
* 2	AU EE	L
* 64	LINE MUTE	L
* 10	$\overline{\text{AFM MUTE}}$	L
* 12	NORM MUTE	L
* 8	BIAS CONT	H
* 9	AFM REC	L
* 63	REC	L
* 22	LIM PL S	L
* 23	LIM PL H	L
* 24	UNBRK PL S	
* 27	UNBRK PL H	
* 28	PINCH PL S	
* 29	PINCH PL H	
* 13	$\overline{\text{VD INT}}$	H
* 4	V MUTE	L
* 3	MC	L
* 60	H SEARCH	L
4	PB TRACON	L
12	FR ON	
15	AFC INH	
63	RESET 194	
> 49	VD/CTL	
> 48	RF SW P	
●	STILL	

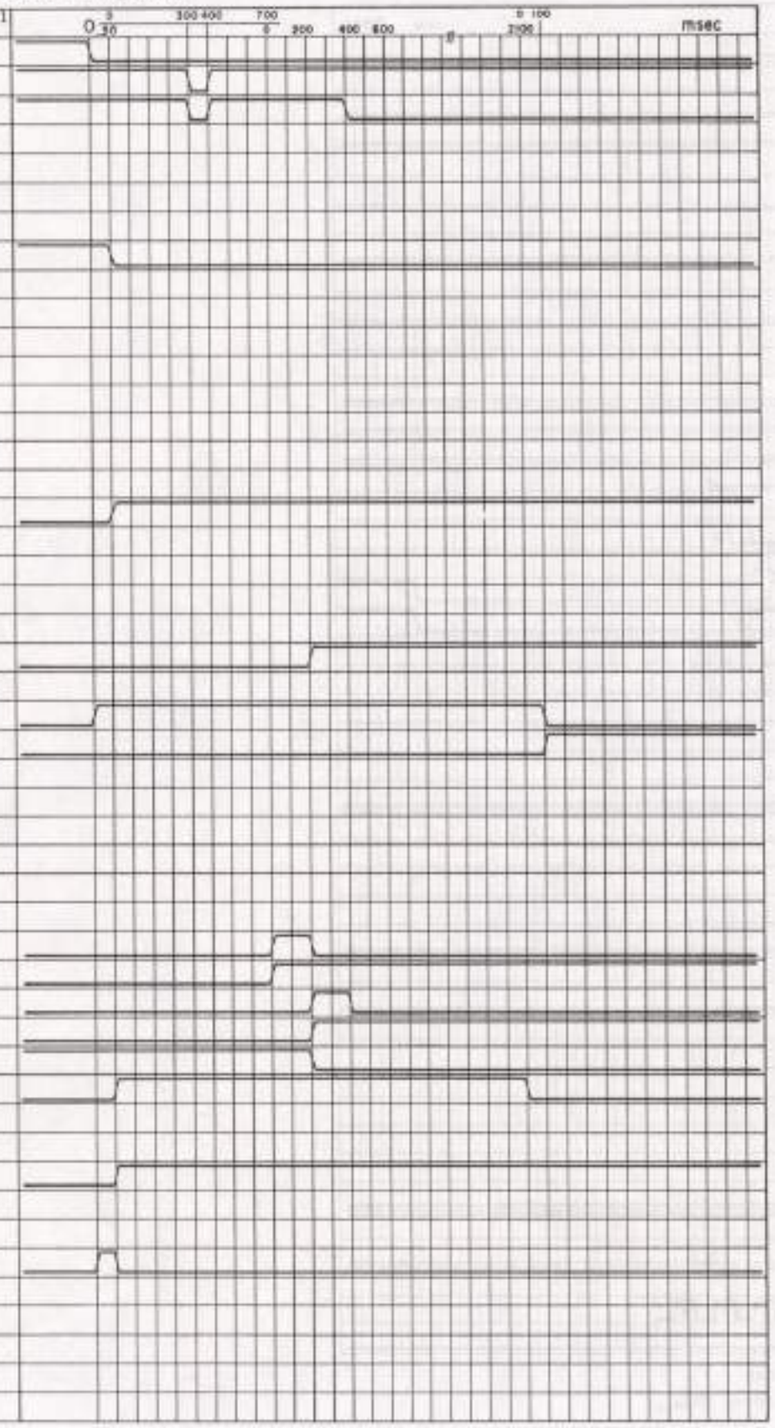


* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal
○ : MECH CON → MCC communications data

Fig. 2-14

1. STOP → PB Mode Transition Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	
20	REEL FWD	
21	REEL STOP	
22	FF/REW(R)	L
23	REEL LOW	H
24	C/R(R)	L
27	CAP FWD	H
5	CAP STOP	
2	$\overline{\text{C/R(C)}}$	H
3	x2	L
11	$\overline{\text{FG MASK}}$	H
64	CTL GAIN	L
62	TOP/$\overline{\text{END}}$	L
28	SLOW	L
29	STEP	L
7	REC·$\overline{\text{P}}$	L
41	V PB	
42	V REC	L
43	PRE REC	L
53	$\overline{\text{A FE}}$	H
52	$\overline{\text{B FE}}$	H
* 1	NORM PB	
* 2	AU EE	L
* 64	LINE MUTE	
* 10	$\overline{\text{AFM MUTE}}$	
* 12	NORM MUTE	L
* 8	$\overline{\text{BIAS CONT}}$	H
* 9	AFM REC	L
* 11	AU INS	L
* 22	LIM PL S	L
* 23	LIM PL H	L
* 24	UNBRK PL S	
* 27	UNBRK PL H	
* 28	PINCH PL S	
* 29	PINCH PL H	
* 13	$\overline{\text{VD INT}}$	
* 4	V MUTE	
* 3	MC	L
* 60	H SEARCH	L
4	PB TRACON	
12	FR ON	L
15	AFC INH	L
63	RESET 194	
> 49	VD/CTL	
> 48	RF SW P	



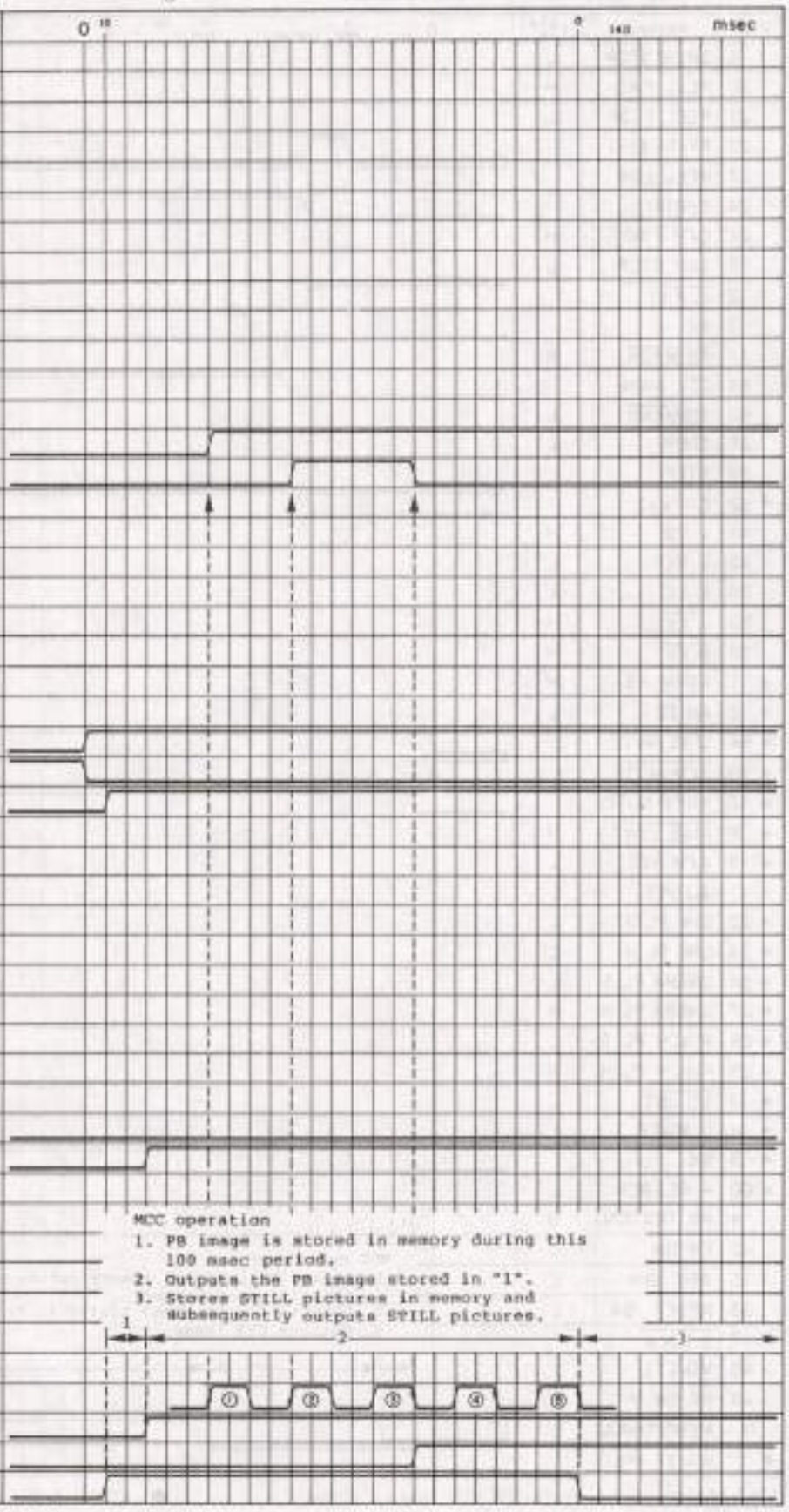
* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal

Fig. 2-13

MEMO

3. PB → PB PAUSE Mode Transition Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	L
20	REEL FWD	H
21	REEL STOP	L
22	FF/REW(R)	L
23	REEL LOW	H
24	C/R(R)	L
27	CAP FWD	H
5	CAP STOP	L
2	$\overline{C/R(C)}$	H
3	x2	L
11	$\overline{FG\ MASK}$	H
64	CTL GAIN	L
62	TOP/$\overline{END}$	L
26	SLOW	
29	STEP	
7	REC·$\overline{P}$	L
41	V PB	X
42	V REC	L
43	PRE REC	L
53	$\overline{A\ FE}$	H
52	$\overline{B\ FE}$	H
* 1	NORM PB	X
* 2	AU EE	L
* 64	LINE MUTE	
* 10	$\overline{AFM\ MUTE}$	
* 12	NORM MUTE	
* 8	$\overline{BIAS\ CONT}$	H
* 9	AFM REC	L
* 11	AU INS	L
* 22	LIM PL S	L
* 23	LIM PL H	L
* 24	UNBRK PL S	L
* 27	UNBRK PL H	H
* 28	PINCH PL S	L
* 29	PINCH PL H	H
* 13	$\overline{VD\ INT}$	L
* 4	V MUTE	
* 3	MC	
* 60	H SEARCH	L
4	PB TRACON	H
12	FR ON	L
15	AFC INH	L
63	RESET 194	L
> 17	$\overline{D\ LOCK}$	
> 49	VD/CTL	
> 48	RF SW P	
○	MEMO/THROU	
●	STILL	
●	WRITE DIS	

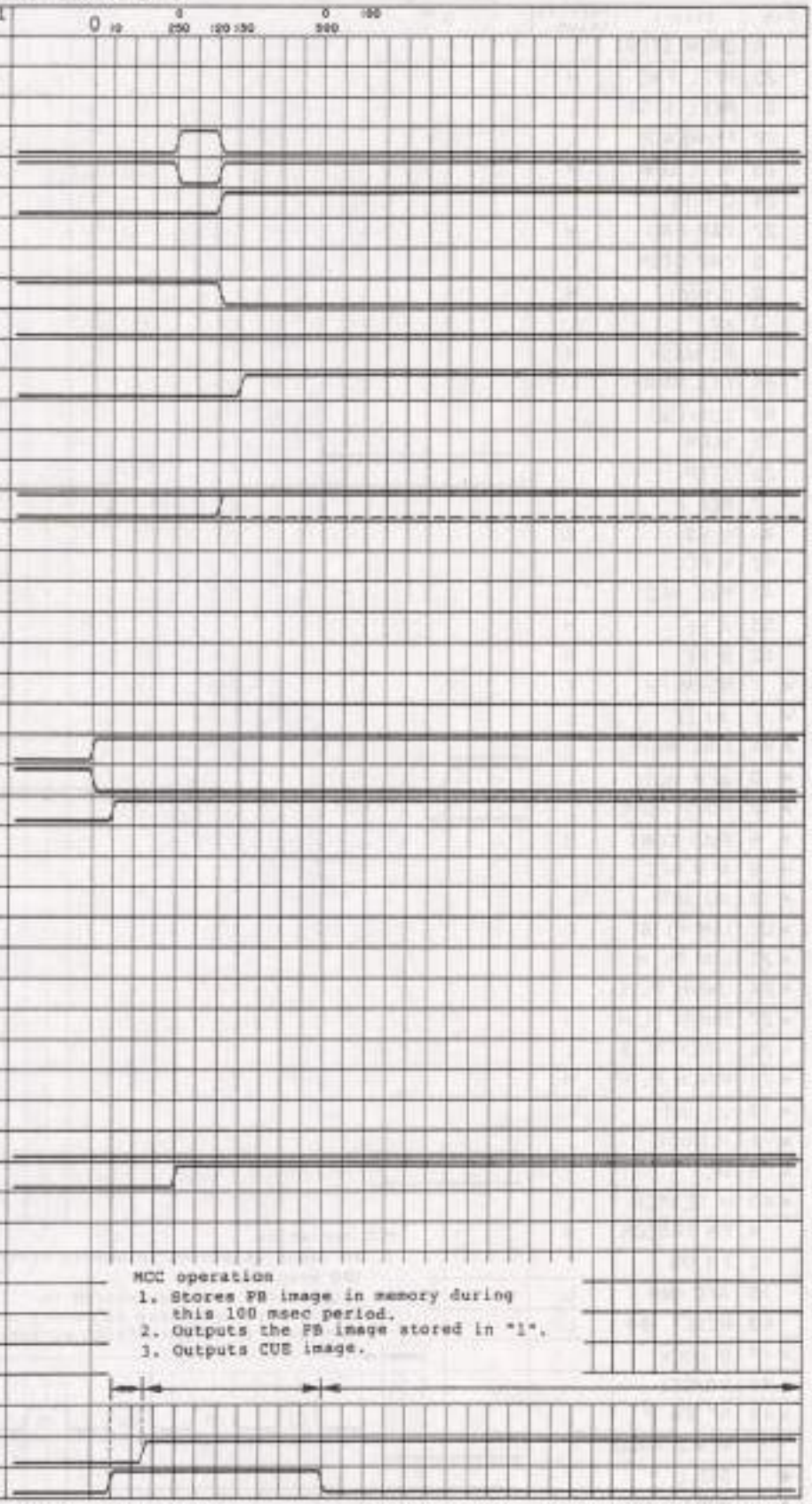


* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal
● : MECH CON → SLOW microcomputer communications data
○ : MECH CON → MCC communications data

Fig. 2-15

4. PB → CUE Mode Transition Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	L
20	REEL FWD	H
21	REEL STOP	L
22	FF/REW(R)	
23	REEL LOW	
24	C/R(R)	
27	CAP FWD	H
5	CAP STOP	L
2	$\overline{C/R(C)}$	
3	x2	
11	$\overline{FG\ MASK}$	H
64	CTL GAIN	
62	TOP/$\overline{END}$	L
28	SLOW	L
29	STEP	L
* 52	C/R+x2	
41	V PB	H
42	V REC	L
50	V EE	L
53	$\overline{A\ FE}$	H
52	$\overline{B\ FE}$	H
* 1	NORM PB	H
* 2	AU EE	L
* 64	LINE MUTE	
* 10	$\overline{AFM\ MUTE}$	
* 12	NORM MUTE	
* 8	$\overline{BIAS\ CONT}$	H
* 9	AFM REC	L
* 11	AU INS	L
* 22	LIM PL S	L
* 23	LIM PL H	L
* 24	UNBRK PL S	L
* 27	UNBRK PL H	H
* 28	PINCH PL S	L
* 29	PINCH PL H	H
* 13	$\overline{VD\ INT}$	L
* 4	V MUTE	
* 3	MC	
* 60	H SEARCH	L
4	PB TRACON	H
12	FR ON	L
15	AFC INH	L
63	RESET 194	L
> 17	$\overline{D\ LOCK}$	
> 49	VD/CTL	
> 48	RF SW P	
○	MEMO/THROU	
●	WRITE DIS	

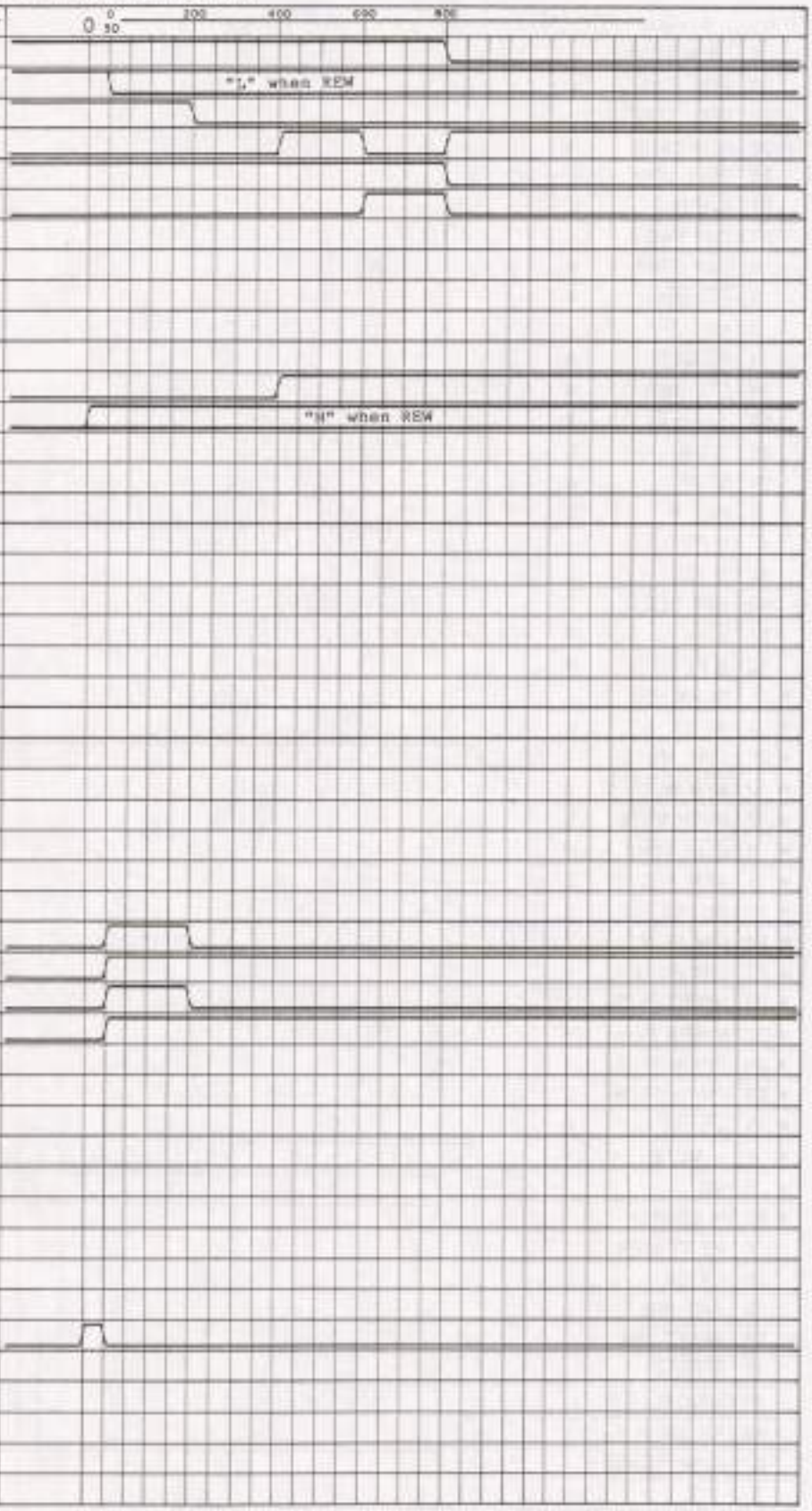


* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal
● : MECH CON → SLOW microcomputer communications data
○ : MECH CON → MCC communications data

Fig. 2-16

5. STOP → FF/REW Mode Transition Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	
20	REEL FWD	
21	REEL STOP	
22	FF/REW(R)	
23	REEL LOW	
24	C/R(R)	
27	CAP FWD	H
5	CAP STOP	H
2	$\overline{\text{C/R(C)}}$	H
3	x2	L
11	$\overline{\text{FG MASK}}$	H
64	CTL GAIN	
62	TOP/$\overline{\text{END}}$	
28	SLOW	L
29	STEP	L
7	REC·$\overline{\text{P}}$	L
41	V PB	L
42	V REC	L
43	PRE REC	L
53	$\overline{\text{A FE}}$	H
52	$\overline{\text{B FE}}$	H
* 1	NORM PB	L
* 2	AU EE	L
* 64	LINE MUTE	L
* 10	$\overline{\text{AFM MUTE}}$	L
* 12	NORM MUTE	L
* 8	$\overline{\text{BIAS CONT}}$	H
* 9	AFM REC	L
* 11	AU INS	L
* 22	LIM PL S	
* 23	LIM PL H	
* 24	UNBRK PL S	
* 27	UNBRK PL H	
* 28	PINCH PL S	L
* 29	PINCH PL H	L
* 13	$\overline{\text{VD INT}}$	H
* 4	V MUTE	L
* 3	MC	L
* 60	H SEARCH	L
4	PB TRACON	L
12	FR ON	L
15	AFC INH	L
63	RESET 194	
> 17	$\overline{\text{D LOCK}}$	
> 49	VD/CTL	
> 48	RF SW P	

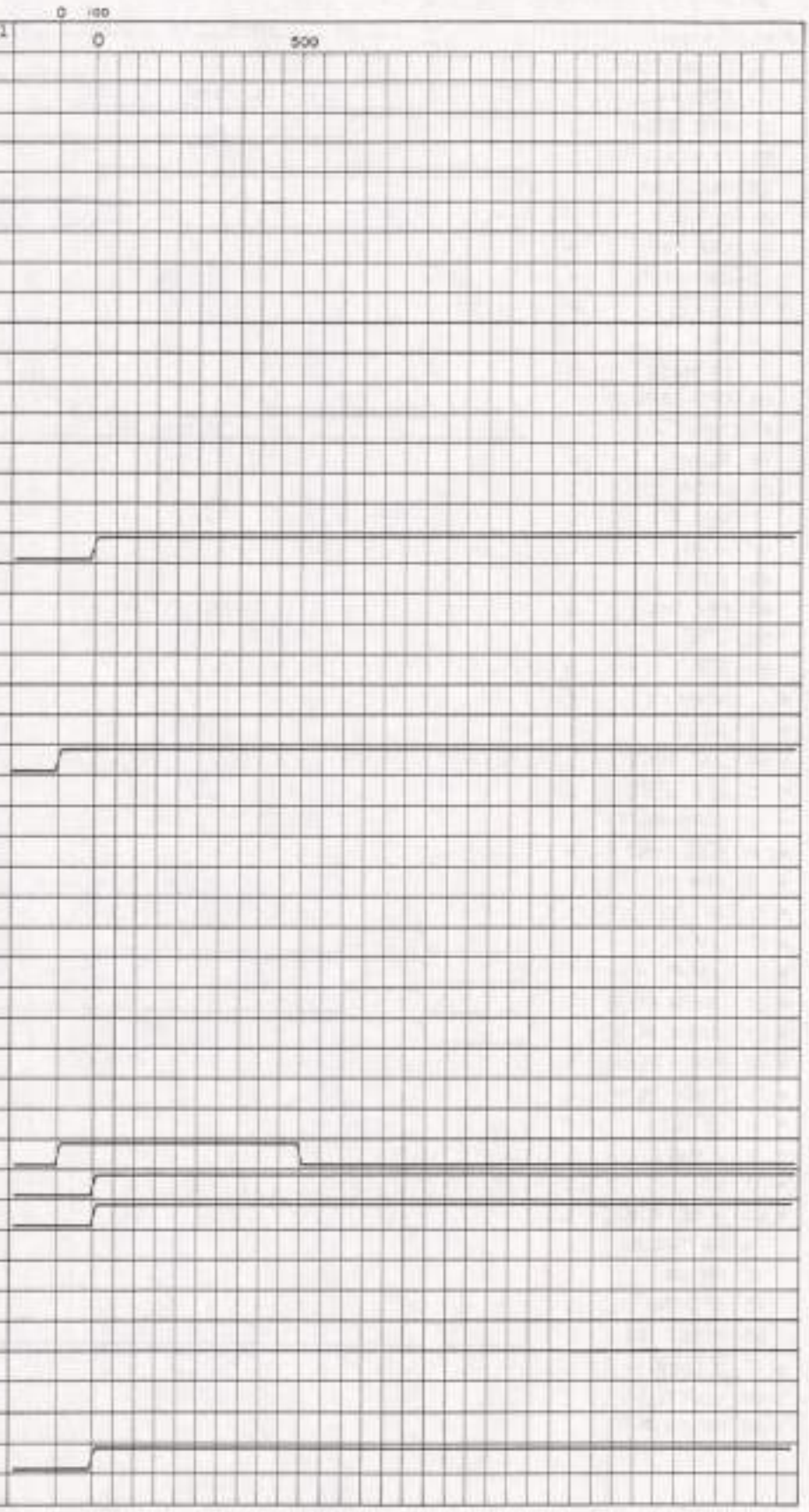


* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal

Fig. 2-17

6. FF/REW → DIGITAL SCAN Mode Transition Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	L
20	REEL FWD	X
21	REEL STOP	L
22	FF/REW(R)	H
23	REEL LOW	L
24	C/R(R)	L
27	CAP FWD	H
5	CAP STOP	H
2	$\overline{\text{C/R(C)}}$	H
3	x2	L
11	$\overline{\text{FG MASK}}$	H
64	CTL GAIN	H
62	TOP/$\overline{\text{END}}$	X
28	SLOW	L
29	STEP	L
7	REC·$\overline{\text{P}}$	L
41	V PB	
42	V REC	L
43	PRE REC	L
53	$\overline{\text{A FE}}$	H
52	$\overline{\text{B FE}}$	H
* 1	NORM PB	L
* 2	AU EE	L
* 64	LINE MUTE	
* 10	$\overline{\text{AFM MUTE}}$	L
* 12	NORM MUTE	L
* 8	$\overline{\text{BIAS CONT}}$	H
* 9	AFM REC	L
* 11	AU INS	L
* 22	LIM PL S	L
* 23	LIM PL H	H
* 24	UNBRK PL S	L
* 27	UNBRK PL H	H
* 28	PINCH PL S	L
* 29	PINCH PL H	L
* 13	$\overline{\text{VD INT}}$	H
* 4	V MUTE	
* 3	MC	
* 60	H SEARCH	
4	PB TRACON	L
12	FR ON	L
15	AFC INH	L
63	RESET 194	L
> 17	$\overline{\text{D LOCK}}$	
> 49	VD/CTL	
> 48	RF SW P	
○	MEMO/$\overline{\text{THROU}}$	

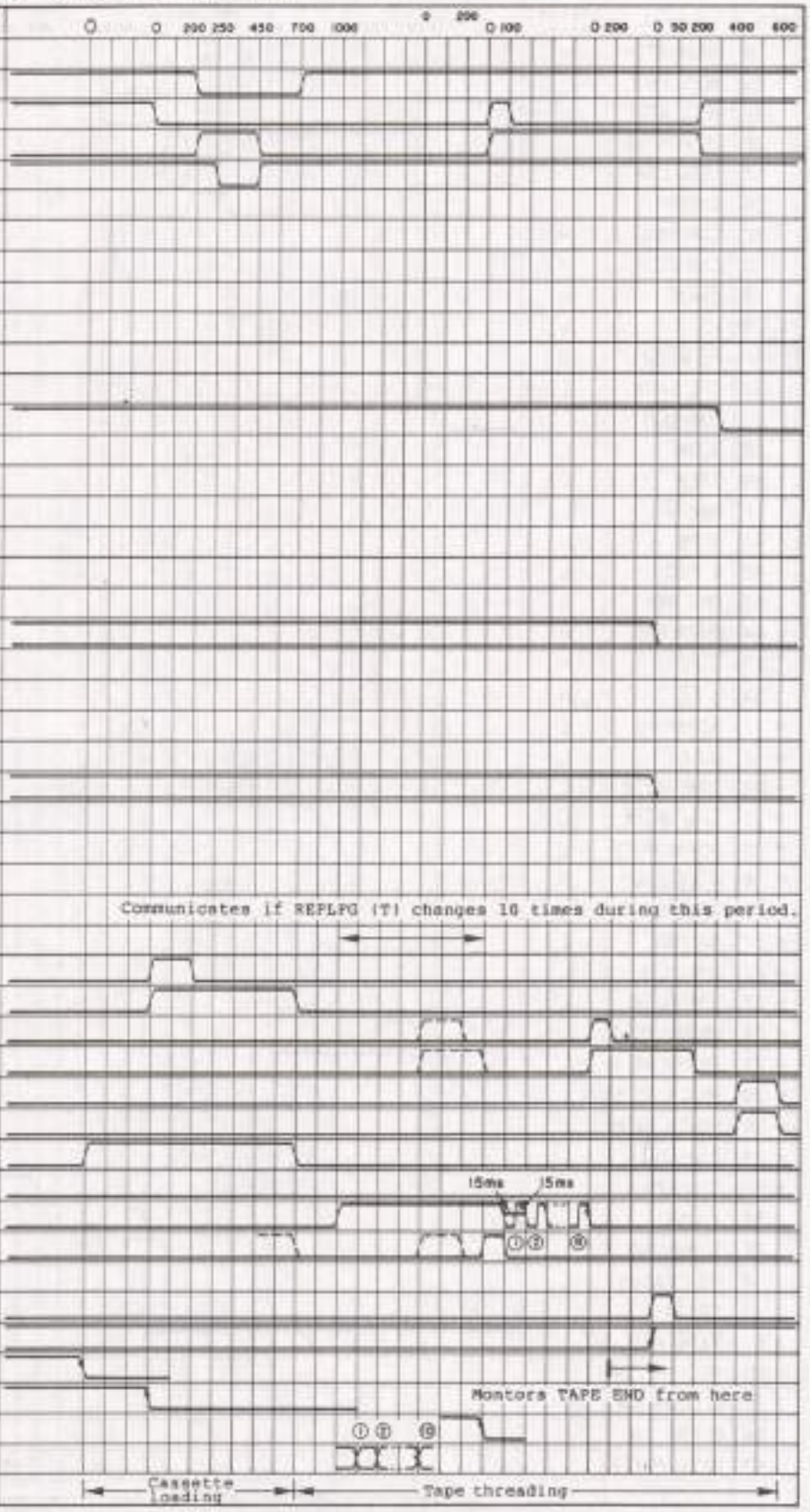


* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal
○ : MECH CON → MCC communications data

Fig. 2-18

7. Cassette Loading and Tape Threading Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	H
20	REEL FWD	
21	REEL STOP	
22	FF/REW(R)	
23	REEL LOW	
24	C/R(R)	L
27	CAP FWD	H
5	CAP STOP	H
2	$\overline{\text{C/R(C)}}$	H
3	x2	L
11	$\overline{\text{FG MASK}}$	H
64	CTL GAIN	L
62	TOP/$\overline{\text{END}}$	
28	SLOW	L
29	STEP	L
7	REC·$\overline{\text{P}}$	L
41	V PB	L
42	V REC	L
43	PRE REC	L
* 4	V MUTE	
53	$\overline{\text{A FE}}$	H
52	$\overline{\text{B FE}}$	H
* 1	NORM PB	L
* 2	AU EE	L
* 64	LINE MUTE	
* 10	$\overline{\text{AFM MUTE}}$	L
* 12	NORM MUTE	L
* 8	$\overline{\text{BIAS CONT}}$	H
* 9	AFM REC	L
* 11	AU INS	L
* 22	LIM PL S	
* 23	LIM PL H	
* 24	UNBRK PL S	
* 27	UNBRK PL H	
* 28	PINCH PL S	
* 29	PINCH PL H	
* 38	C LOAD	
* 37	C UNLOAD	
38	T LOAD	
37	T UNLOAD	
4	PB TRACON	L
63	RESET 194	
> 61	$\overline{\text{TAPE END}}$	
> 60	REC PRF SW	
> 35	C DOWN SW	
> 56	L END SW	
> 47	REEL FG(T)	

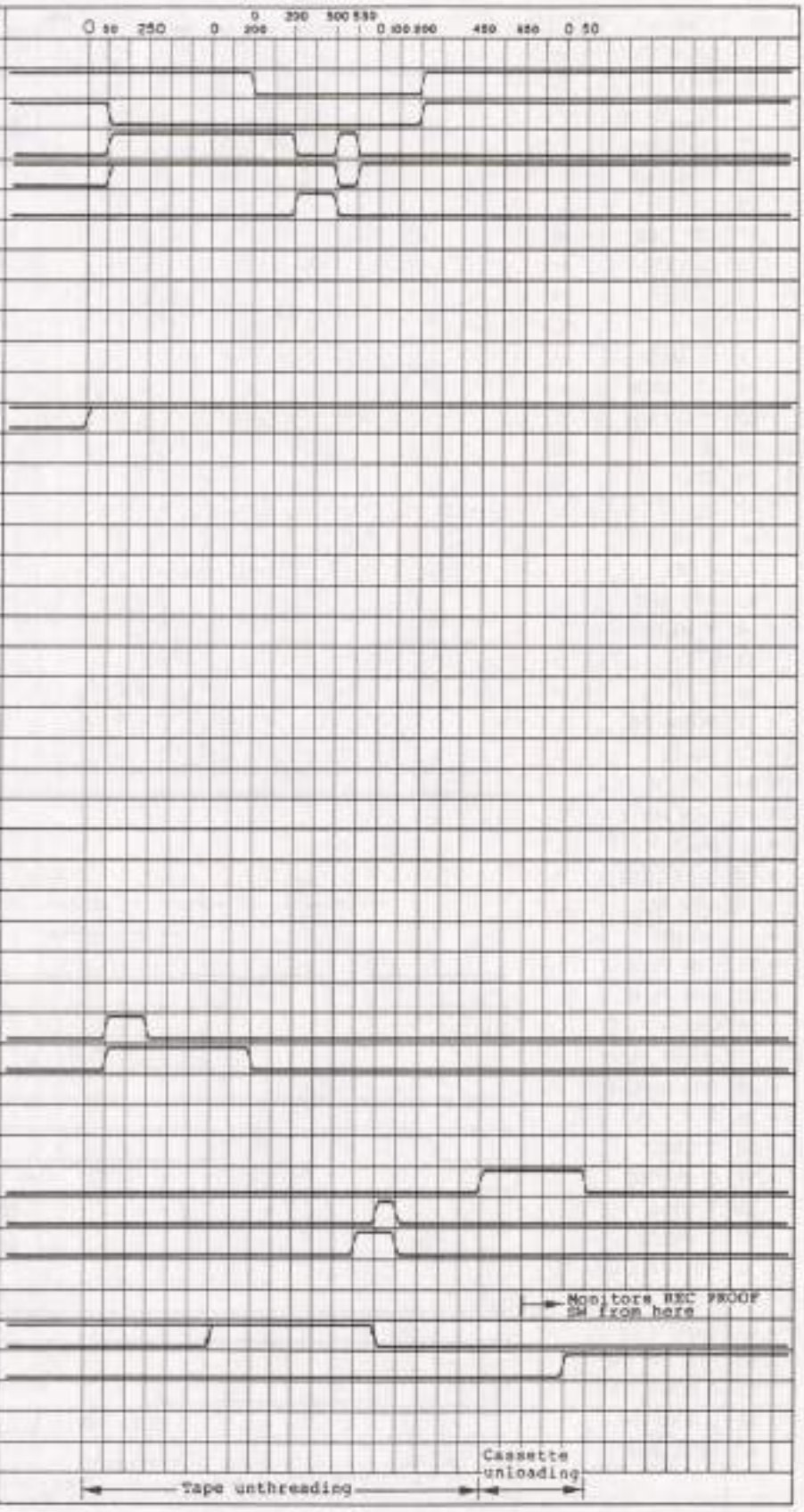


* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal

Fig. 2-19

8. EJECT (Tape Unthreading, Cassette Unloading) Timing Chart

PIN	Signal	Initial value
6	DRUM STOP	H
20	REEL FWD	
21	REEL STOP	
22	FF/REW(R)	
23	REEL LOW	
24	C/R(R)	
27	CAP FWD	H
5	CAP STOP	H
2	$\overline{\text{C/R(C)}}$	H
3	x2	L
11	$\overline{\text{FG MASK}}$	H
64	CTL GAIN	L
62	TOP/$\overline{\text{END}}$	
28	SLOW	L
29	STEP	L
7	REC $\overline{\text{P}}$	L
41	V PB	L
42	V REC	L
43	PRE REC	L
44	OVER REC	H
53	$\overline{\text{A FE}}$	H
52	$\overline{\text{B FE}}$	H
* 1	NORM PB	L
* 2	AU EE	L
* 64	LINE MUTE	L
* 10	$\overline{\text{AFM MUTE}}$	L
* 12	NORM MUTE	L
* 8	$\overline{\text{BIAS CONT}}$	H
* 9	AFM REC	L
* 11	AU INS	L
* 22	LIM PL S	L
* 23	LIM PL H	L
* 24	UNBRK PL S	
* 27	UNBRK PL H	
* 28	PINCH PL S	L
* 29	PINCH PL H	L
* 38	C LOAD	L
* 37	C UNLOAD	
38	T LOAD	
37	T UNLOAD	
4	PB TRACON	L
12	FR ON	L
> 61	$\overline{\text{TAPE END}}$	
> 60	REC PRF SW	
> 35	C DOWN SW	
> 56	L END SW	
> 47	REEL FG(T)	



* : SLOW microcomputer (IC402) output signal
Unmarked : MECH CON (IC401) output signal
> : MECH CON (IC401) input signal

Fig. 2-20

2-3. SLOW MICROCOMPUTER

The SLOW microcomputer has the following six functions.

1. SLOW control
2. Remaining tape display
3. INDEX write and erase
4. Port output of data from MECH CON
5. Pseudo CTL output
6. Pseudo VD output

2-3-1. SLOW Control

In SLOWcontrol, the SLOW microcomputercontrols the capstan motor in place of the servo IC.

1. The mode control judges whether there is a mode transition from function switch, JOG & SHUTTLE and remote control information, and notifies MECH CON by serial communication if there is a mode transition.
2. If MECH CON judges that SLOW control is necessary in that mode transition, it outputs STEP pulses (pulse of about 50 msec output from Pin ㊸) timed with RF SW pulse rise to the SLOW microcomputer.
3. The SLOWmicrocomputerdetermines what SLOW control to execute of the six SLOW controls from the three signal levels of CAP FWD (Pin ㊶), SLOW (Pin ㊷) and STILL (Internal communications data during startup of the STEP pulse (Pin ㊸), and executes that control. The types of CAP FWD, SLOW and STILL signals are as follows.

CAP FWD	SLOW	STILL	SLOW Control	Principal Uses
H	L	H	STILL → PB	STILL → PB (×1)
L	L	H	STILL → −×1	STILL → −×1
H	H	L	PB → STILL	PB (×1) → STILL
L	H	L	−× → STILL	−×1 → STILL
H	H	H	STILL → FWD → STILL	FWD SLOW
L	H	H	STILL → RVS → STILL	RVS SLOW

Table 2-5

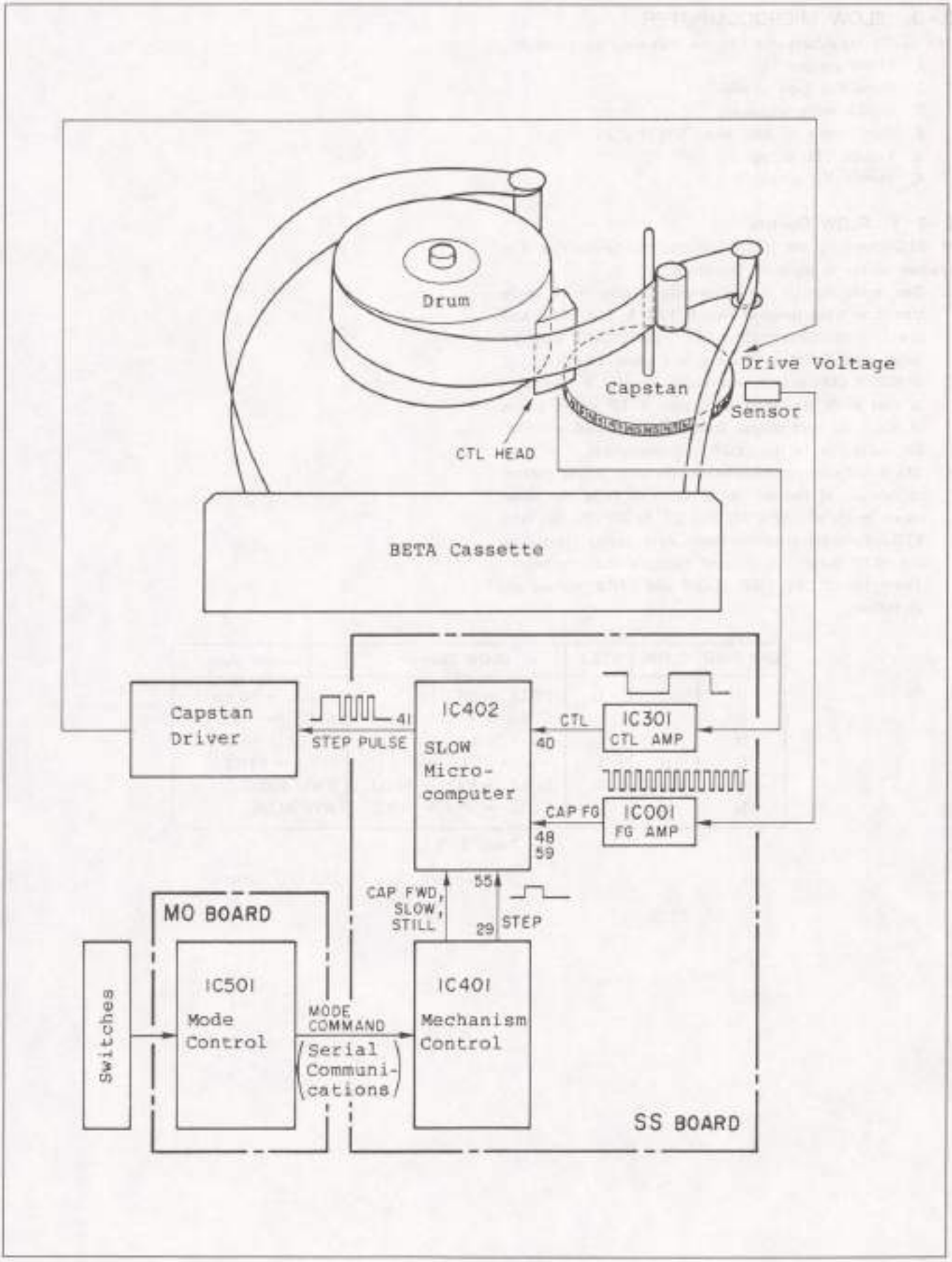


Fig. 2-21 Basic SLOW control block diagram

1. STILL → PB Timing Chart

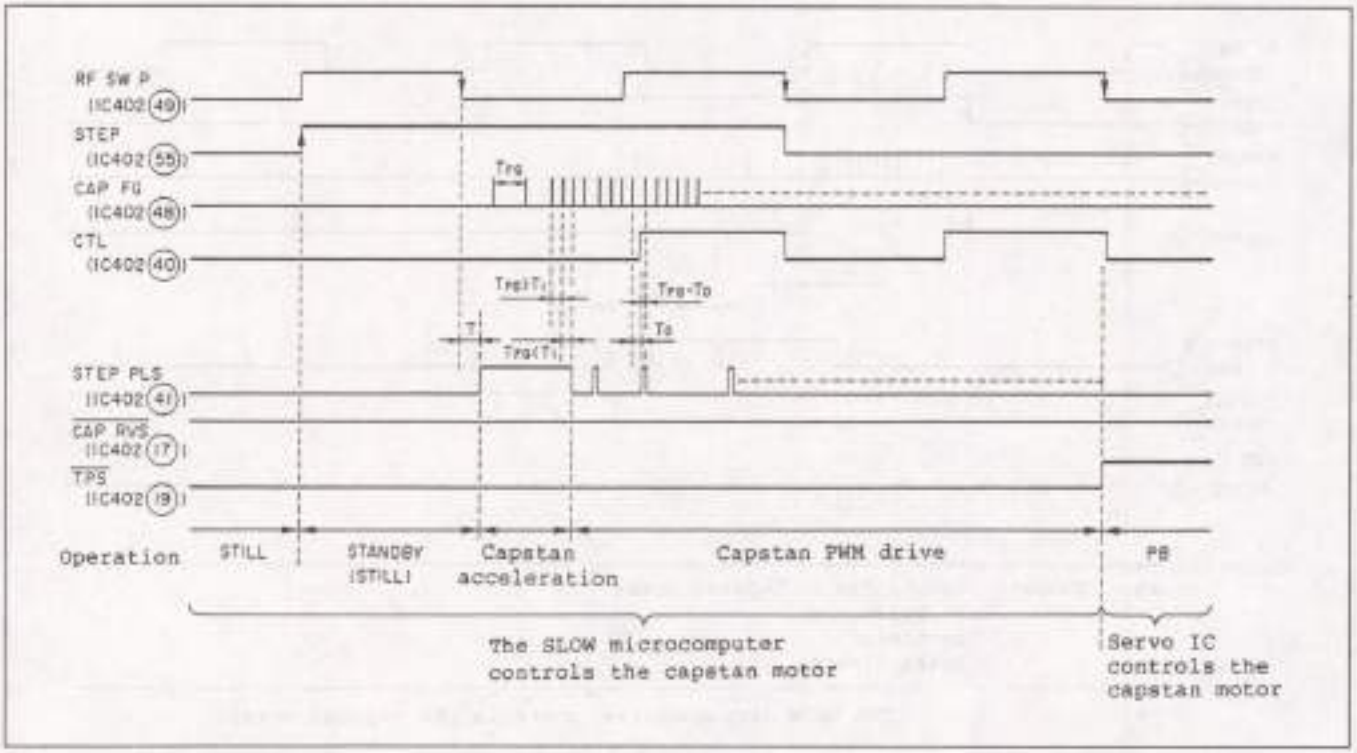


Fig. 2-22

2. STILL → −×1 Timing Chart

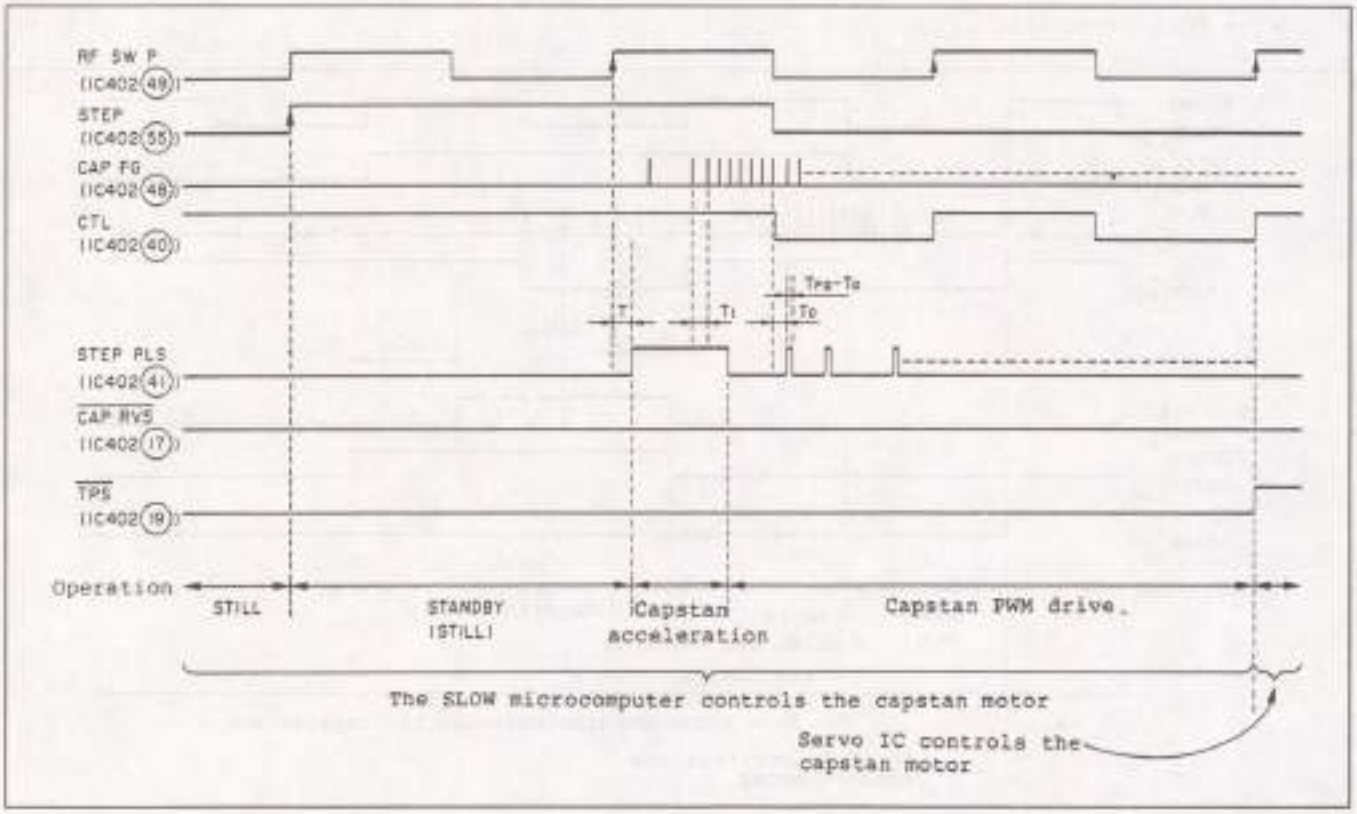


Fig. 2-23

3. PB → STILL Timing Chart

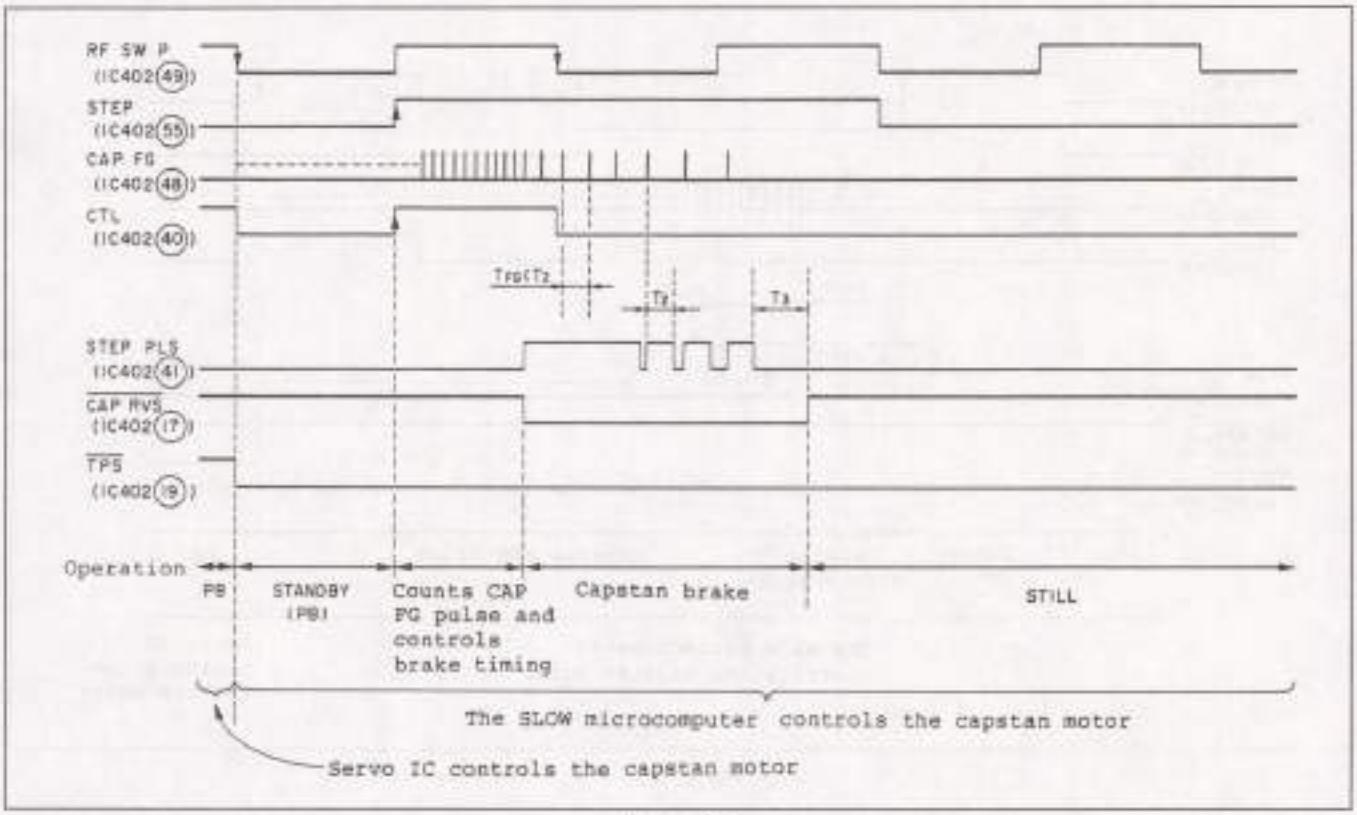


Fig. 2-24

4. −×1 → STILL Timing Chart

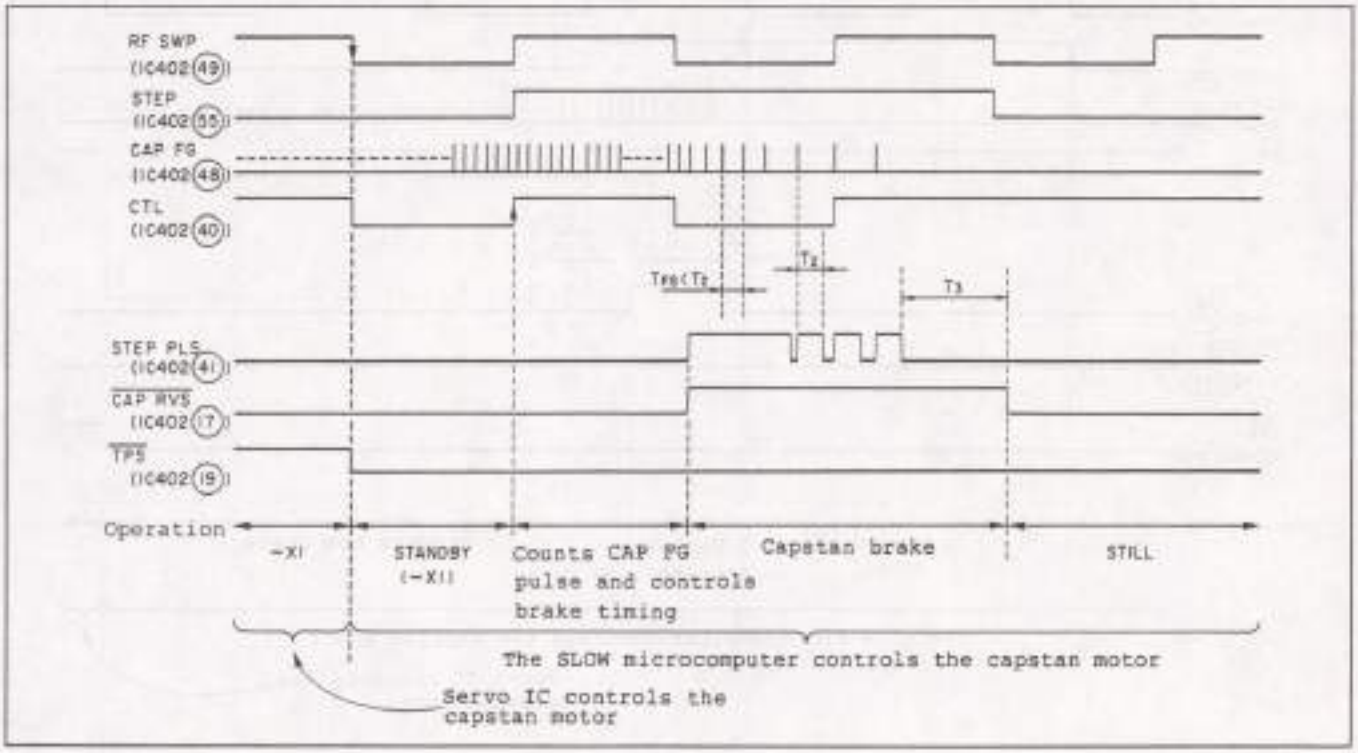


Fig. 2-25

5. STILL → FWD → STILL Timing Chart

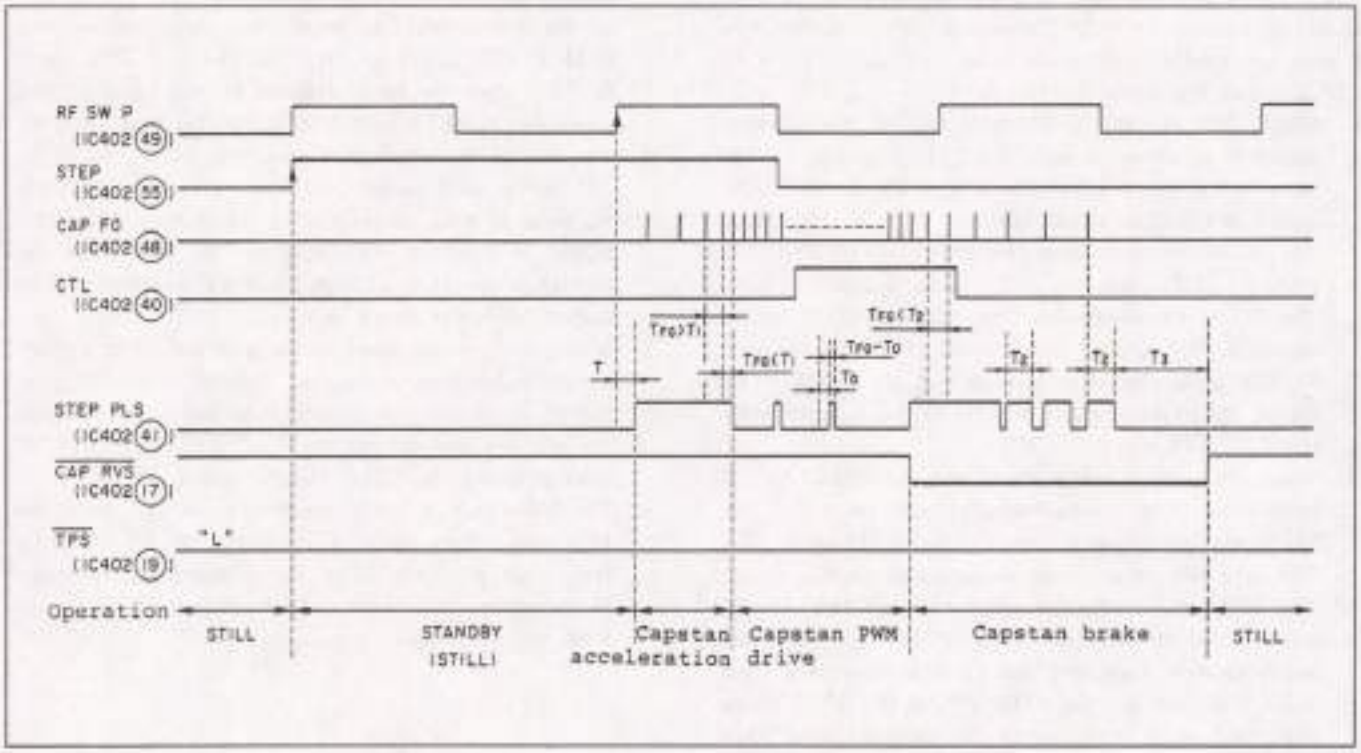


Fig. 2-26

6. STILL → RVS → STILL Timing Chart

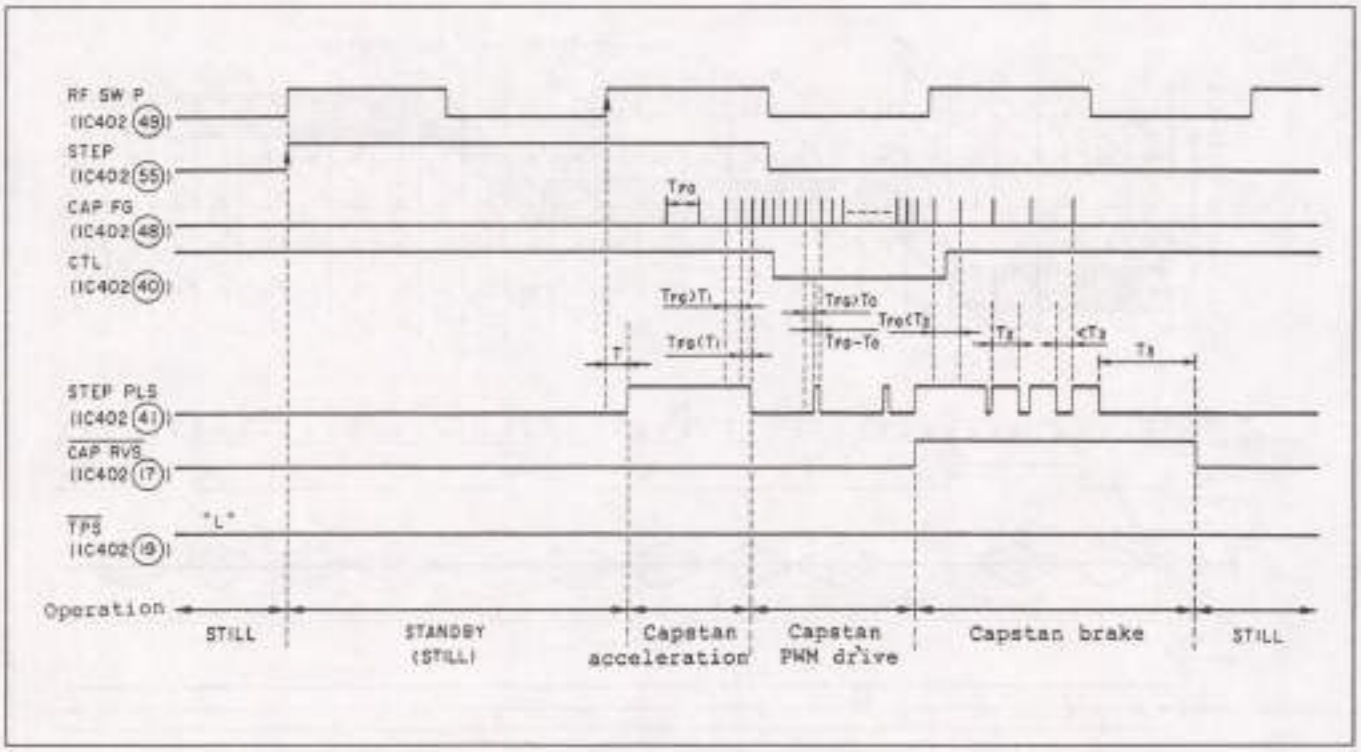


Fig. 2-27

(Actual Example of SLOW Control)

The FWD 1/5 SLOW operation will be explained here as an actual example of SLOW control. In this operation, five frames are operated in synchronism (STILL → FWD → STILL), (See Fig. 2-26 and 2-28.)

1. MECH CON sets the STEP signal to "H" for a 3-field period in synchronism with rise (_|‾) of the RF SW pulse every five frames. The CAP FWD signal, SLOW signal and STILL signal are all "H" at this time. The SLOW microcomputer therefore controls STILL → FWD → STILL each the STEP pulse is input.
2. The SLOW microcomputer first sets the STEP PULSE signal to "H" after a fixed period (T) from the first RF SW pulse rise after startup (_|‾) of the STEP signal. The capstan motor will be driven forward since the $\overline{\text{CAP RVS}}$ signal is "H".
3. When the capstan motor starts and the CAPSTAN FG pulse cycle (T_{FG}) drops below a fixed value (T_1), the SLOW microcomputer returns the STEP PULSE to "L". The tape will be at about single speed at this time.
4. The SLOW microcomputer measures the CAPSTAN FG pulse cycle and sets the STEP PULSE to "H" and accelerates the capstan if the cycle is above the fixed value (T_0) and sets the STEP PULSE to "L" if below this fixed value and reduces the capstan speed. Tape speed is therefore maintained at single speed by this PWM drive.
5. The SLOW microcomputer counts the CAPSTAN FG pulse from startup (_|‾) of the CTL signal and applies reverse brake to the capstan motor and sets the STEP PULSE signal to "H" and the $\overline{\text{CAP RVS}}$ signal to "L" when the count reaches a fixed value (differs according to BETAmode and SLOW Tracking control).
6. The SLOW microcomputer sets the STEP PULSE to "H" for a fixed period (T_2) each time the CAPSTAN FG pulse is input when braking the capstan. The STEP PULSE is therefore maintained at "H" level when the capstan is operating at high speed, and becomes a pulse output when the speed drops.
7. When the capstan speed drops and the STEP PULSE output pulse interval exceeds a fixed value (T3), the SLOW microcomputer judges that the capstan motor has stopped and returns the $\overline{\text{CAP RVS}}$ signal to "H" after stopping the STEP PULSE output.
8. The WE signal of the DI board becomes "L" for a one field period from fall (‾|_) of the 5th RF SW pulse from startup of the STEP signal, and playback image is stored in the memory. This image is then output from the next field.

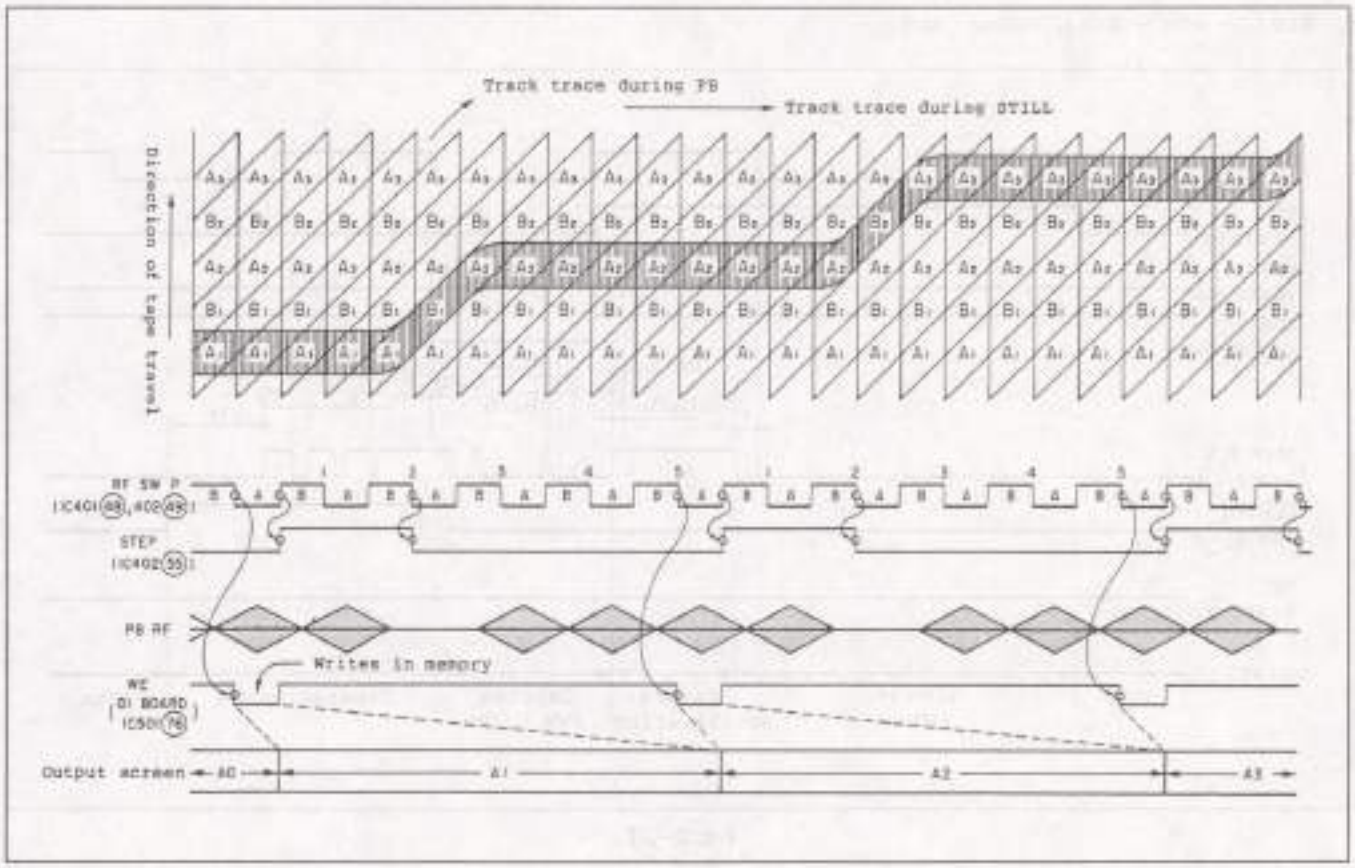


Fig. 2-28 Head locus and output screen in the FWD 1/5 SLOW mode

2-3-2. Remaining Tape Display

The microcomputer measures the rotating cycle of the reel base of both the S and T sides and calculates the remaining amount of tape. Measurement of the rotating cycle and calculation of the remaining tape are as follows.

1. The reel base of both the S and T sides generate 30 pulses for each rotation. The microcomputer obtains the rotating cycle of the reel base from the time required to count 30 of these pulses (REEL FG S (Pin 47) of IC402) on the S side and REEL FG T (Pin 46 of IC402) on the T side).
2. The SLOW microcomputercalculates the remaining tape from the following information.
   1) Rotating cycle of the S reel base
   2) Rotating cycle of the T reel base
   3) BETA Mode (Data transferred from MECH CON)
   4) Tape selector state (Data transferred through the MODE CON and MECH CON)

   The calculated data is transferred to MODE CON through MECH CON. MODE CON transfers this data to the timer microcomputer and the CRT microcomputer. The timer microcomputer dispalys the remaining tape on the fluorescent character display tube and CRT microcomputer displays this on the monitor TV screen.

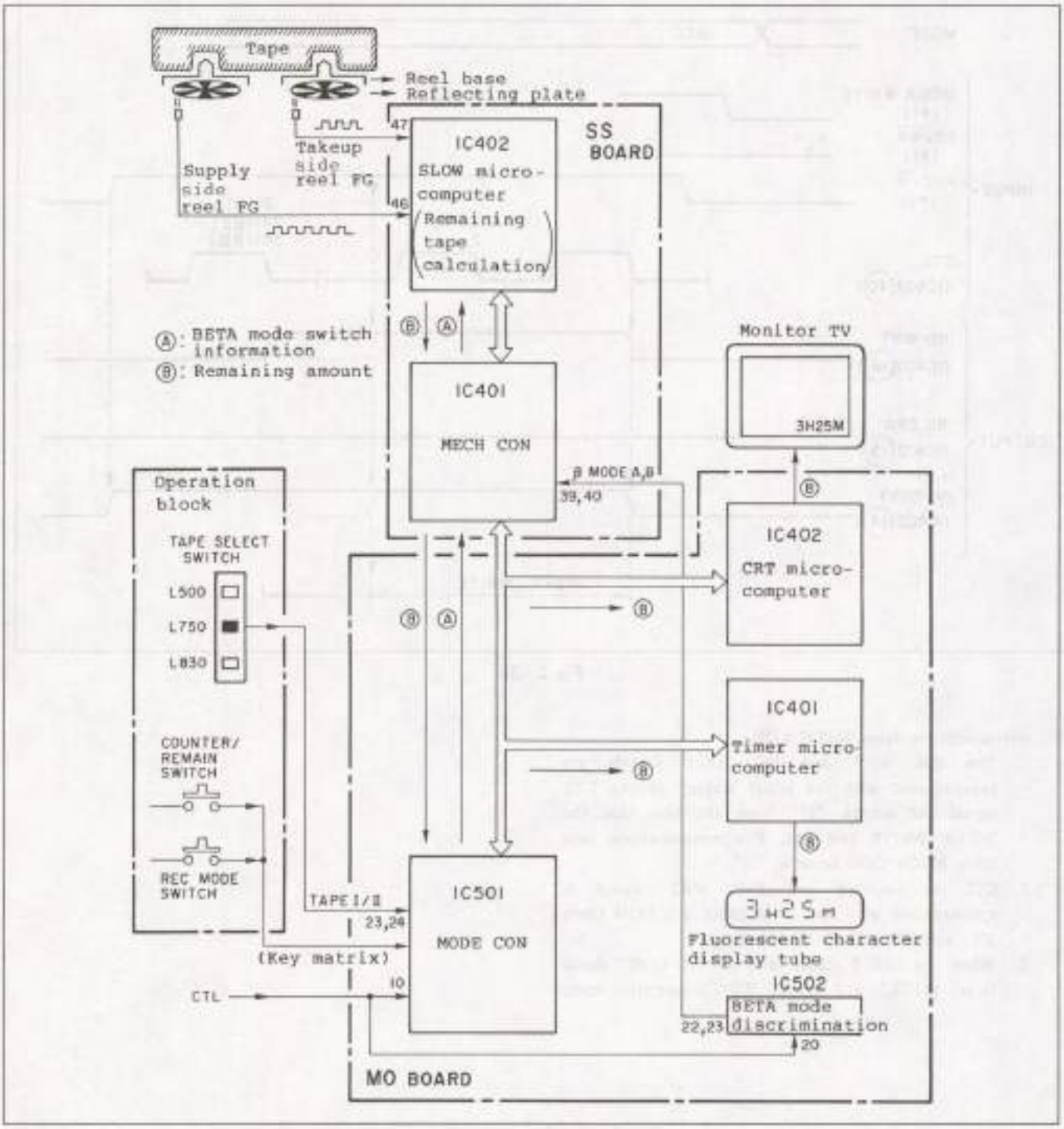


Fig. 2-29 Remaining-tape display block diagram

2-3-3. INDEX Write and Erase

The SLOW microcomputer executes INDEX WRITE and INDEX ERASE by control signals (serial communications data) from MECH CON. The three output signals INDEX WRT, INDEX ERA and HC CONT are generated in synchronism with the CTL signal for this purpose.

(1) INDEX WRITE operation during REC

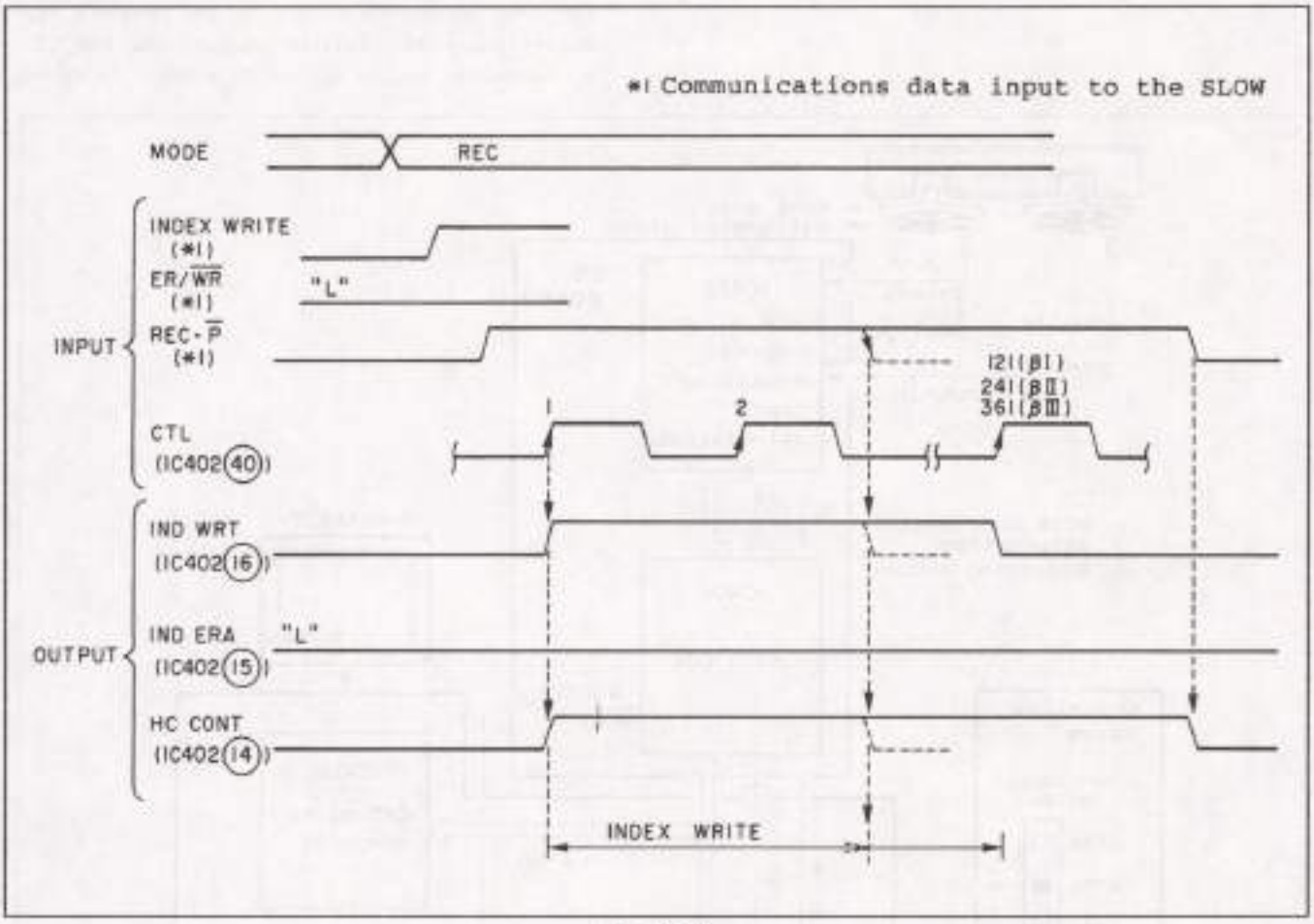


Fig. 2-30

microcomputer from MECH CON

1. The INT WRT and HC CONT signals are synchronized with the initial startup of the CTL signal and set to "H" from the time that the INDEX WRITE and REC P communications data from MECH CON become "H".
2. CTL is counted and IND WRT signal is synchronized with the 121st (Beta I), 241st (Beta II) and 361st (Beta III) rise.
3. When the REC $\overline{P}$ signal falls, the HC CONT signal is set to "L" and INDEX WRITE operation ends.

(2) INDEX WRITE operation during PB

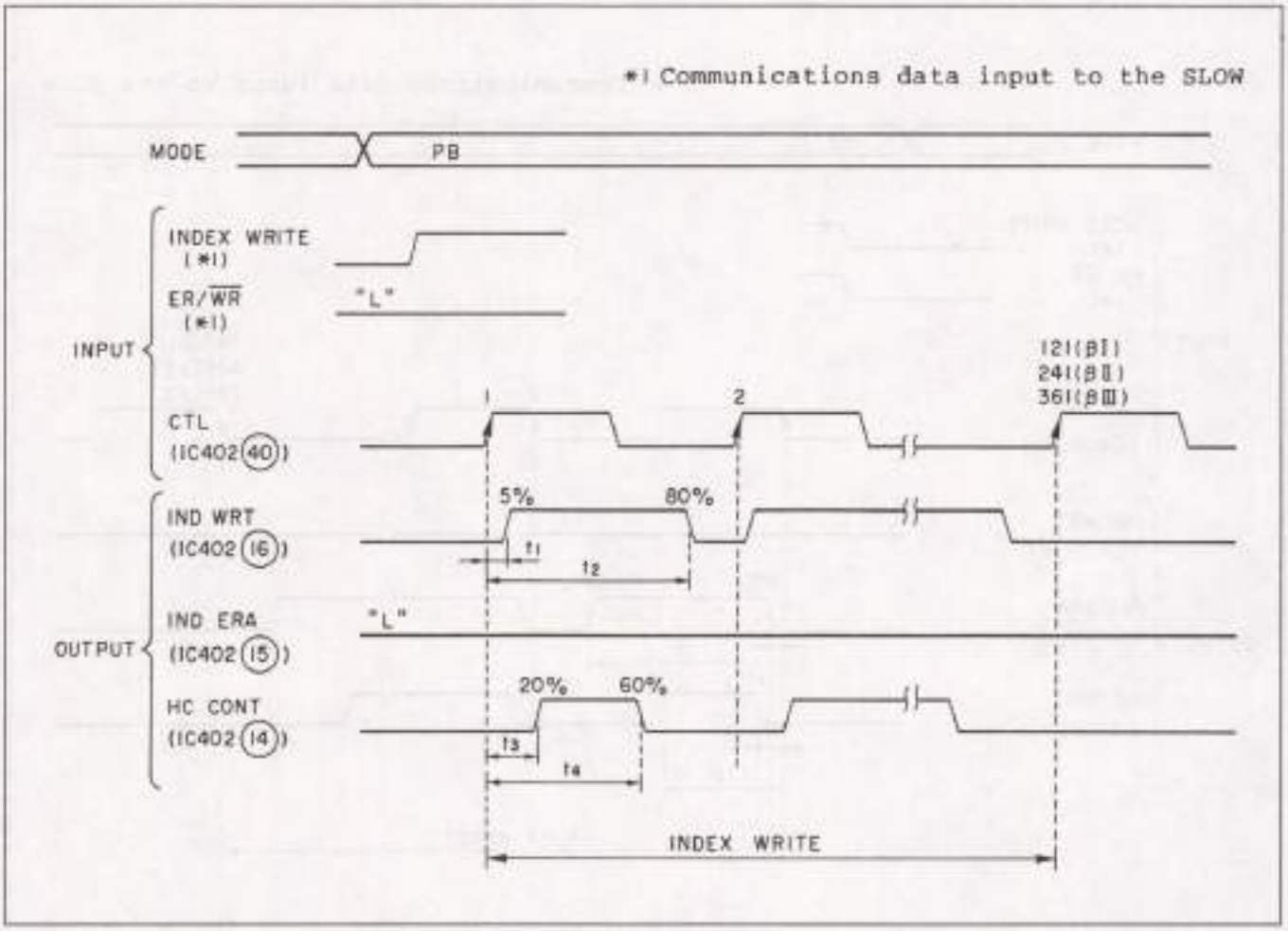


Fig. 2-31

1. Communications data INDEXWRITE from MECH CON becomes "H" and IND WRT and HC CONT signals are output at set times t_1 – t_4 with initiak CTL rise as reference. The same also occurs from the second time on.

   Set time –
   - t1 = 1.7 ms
   - t2 = 26.7 ms
   - t3 = 6.7 ms
   - t4 = 20.0 ms

2. Counts CTL signals and sets both IND WRT and HC CONT signals to "L" after the 121st (Beta I), 241st (Beta II) and 361st (Beta III) counts.

(3) INDEX ERASE operation during PB

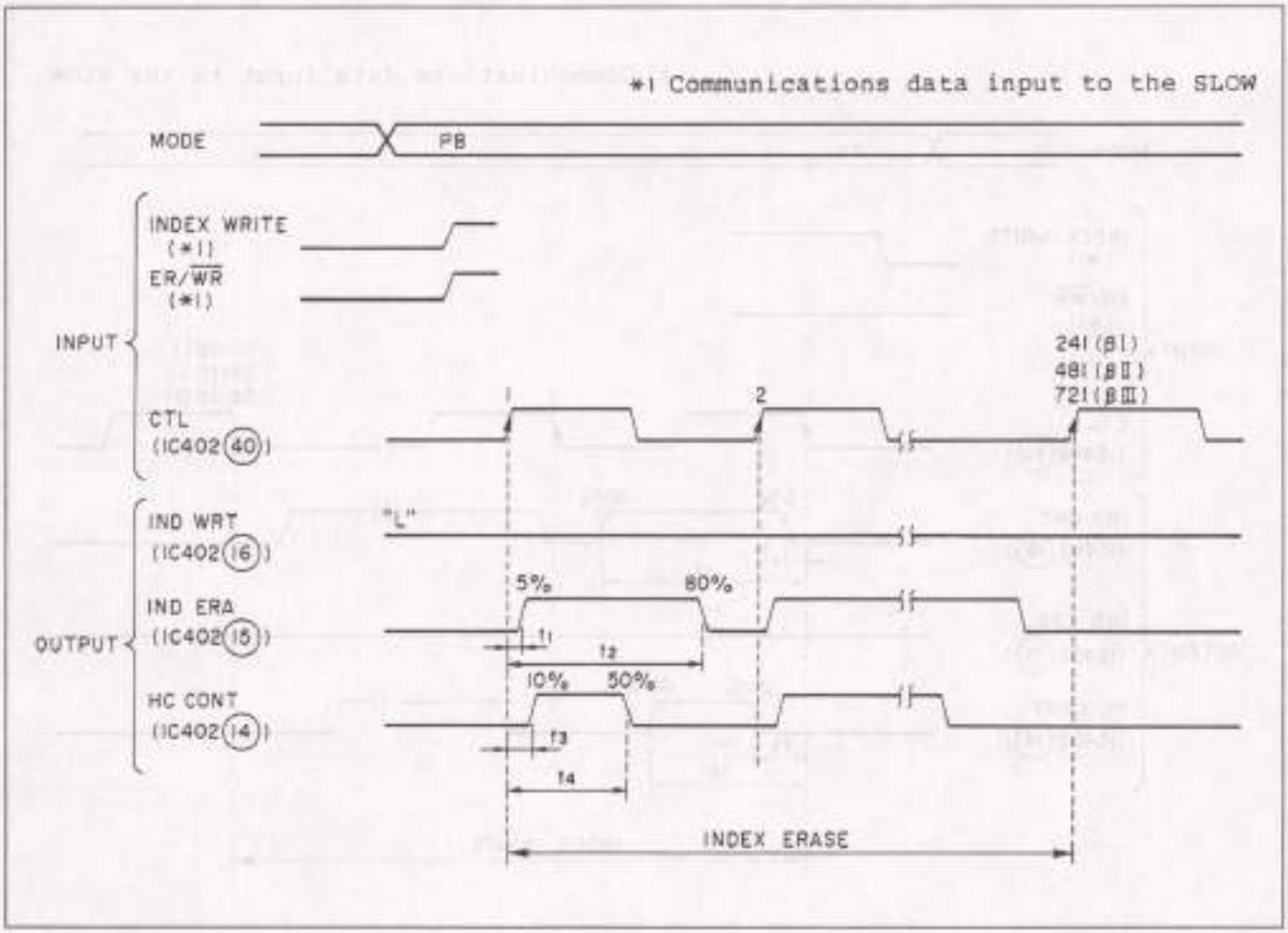


Fig. 2-32

1. Communications data INDEXWRITE and ER/WR from MECH CON become "H" and IND ERA and HC CONT signals are output at set times t_1 – t_4 with initial startup of CTL as reference. The same also occurs from the second time on.

   Set time –
   - t1=1.7 ms
   - t2=28.7 ms
   - t3=3.3 ms
   - t4=16.7 ms

2. Counts the CTL signals and sets both IND ERA and HC CONT signals to "L" after the 241st (Beta I), 481st (Beta II) and 721st (Beta III) counts.

2-3-4. Pseudo CTL Output

If tape speed drops sharply when PB CTL pulses are generated such as in SLOW playback, the CTL pulse of the CTL head output will be small and may not reach the threshold level of the waveform shaping Schmitt amp (IC301). CTL pulses will not be output to system control in this case. MODE CON counts the CTL pulses and displays tape count. If a miscount of the CTL pulses occurs, tape counter accuracy, particularly frame accuracy, will deteriorate. Editing accuracy will also deteriorate.

To prevent this, the SLOW microcomputer creates a pseudo CTL signal by counting the CAPSTAN FG signal during SLOW control and outputs this when the PB CTL signal is not reproduced.

(SLOW/STILL Playback)

Pin ㊾ (SCE) of the SLOW microcomputer becomes "H". This causes Q420 and Q423 to go ON, Q419 to go OFF and the CTL PLS output of Pin ㊿ of the SLOW microcomputer is output to MODE CON through the Q420.

The FC board compensates for that portion that the SLOW microcomputer is unable to compensate for.

(Other modes)

Pin ㊾ (SCE) of the SLOW microcomputer becomes "L". This causes Q420 and Q423 to go OFF and Q419 to go ON. The VD/CTL signal from the amp (IC301) of the servo circuit is output to MODE CON.

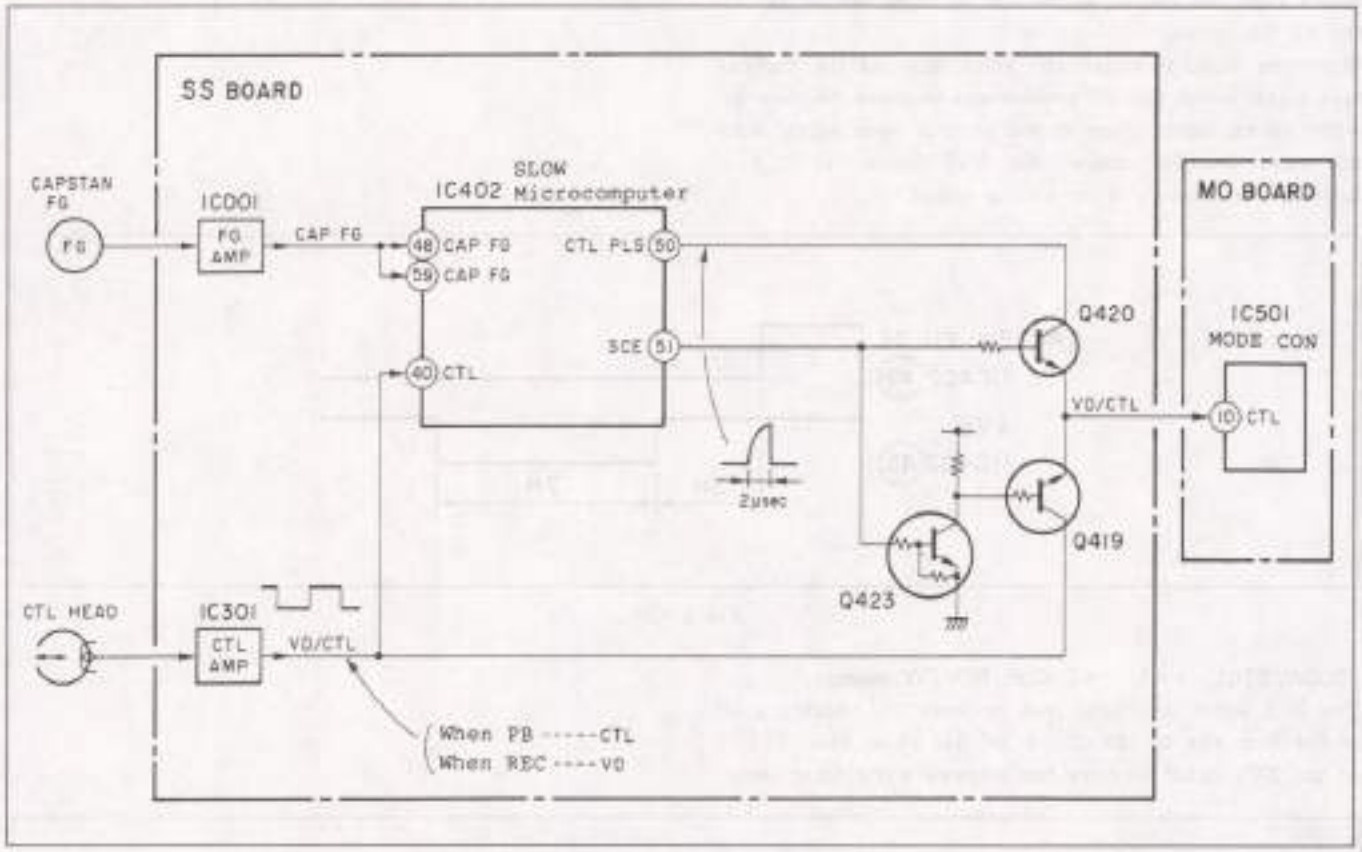


Fig. 2-33 Pseudo CTL circuit

2-3-5. Pseudo VD (XVS) Output

The SLOW microcomputer generates pseudo VD signals (XVS : Pin ㊺ of IC402) as memory timing signals of the playback image. Although a vertical sync signal separated from the playback video signal should primarily be used for writing in memory, noise bars are generated during the vertical blanking period (especially during SLOW/STILL playback) in variable speed playback to improve playback image quality. An XVS signal is therefore generated from the RF SW pulse as a pseudo VD signal during variable speed playback since the vertical sync signal will be disturbed by noise.

(PB, ×1, ×2 Modes)

The XVS signal is a pulse that becomes "L" during the period from the 3rd H to the 7th H from rise or fall of the RF SW pulse.

When the servo is stable, the front edge of the vertical sync signal enters this 7H section and becomes the memory write timing signal. Even if the vertical sync signal does not enter this 7H section, the XVS signal rise (_∫‾) becomes the memory write timing signal.

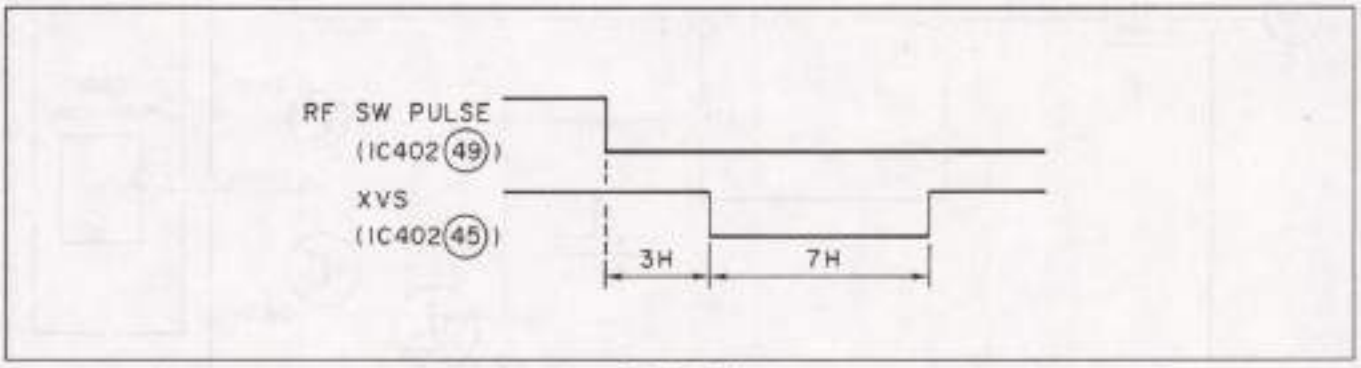


Fig. 2-34

(SLOW, STILL, −×1, −×2, CUE, REVIEW modes)

The XVS signal is a pulse that becomes "L" during a 1H period from rise or fall of the RF SW pulse. Rise (_∫‾) of the XVS signal becomes the memory write timig signal.

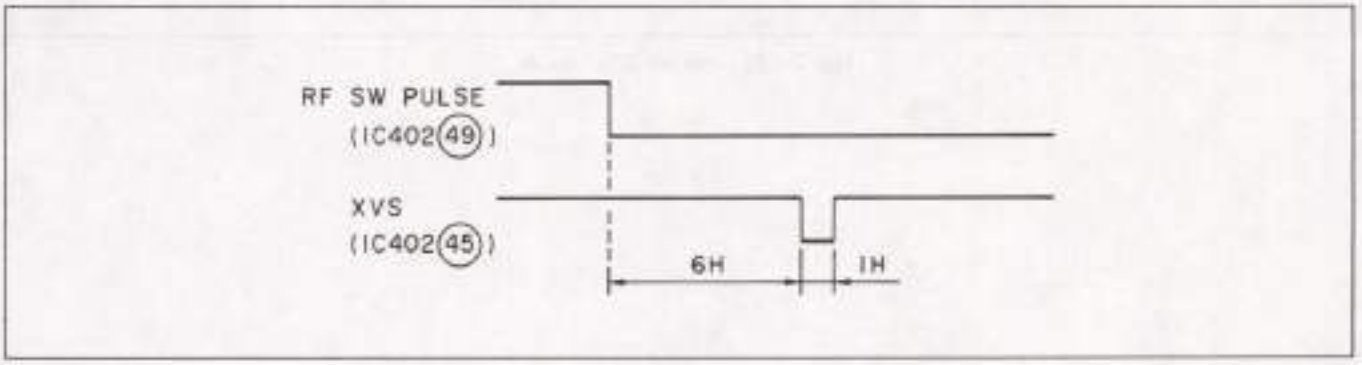


Fig. 2-35

2-3-6. SLOW Microcomputer Terminal Functions

The microcomputer also functions as the expansion output board of MECH CON. The signals marked (*) are communications data output as is from MECH CON.

Terminal No.	Port	Signal	I/O	Function
1	PB1	NORM PB *	O	The normal audio circuit (VE board) becomes "H" in playback state.
2	PB2	AU EE *	O	E-E signal for the audio circuit. Becomes "H" when the EE button is pressed during playback.
3	PB3	MC *	O	Normal playback/variable speed playback switching signal for the audio circuit. "H" during variable speed playback.
4	PE0	V MUTE *	O	Video output mute signal. This signal becomes "H" during transition from STOP to PB and when the CTL signal is not reproduced during normal playback.
5	PE1	$\overline{\beta \text{III}}$	O	"L" in the β III mode.
6	PE2	$\overline{\beta \text{II}}$	O	"L" in the β II mode.
7	PE3	$\overline{\beta \text{I}}$	O	"L" in the β I mode.
8	PF0	$\overline{\text{BIAS CONT}}$ *	O	"L" when REC or INSERT. This signal causes the BIAS/ERASE oscillator circuit to operate.
9	PF1	AFM REC *	O	REC signal for the BETA HIFI audio circuit. "H" when recording BETA HIFI signals (AFM signals).
10	PF2	$\overline{\text{AFM MUTE}}$ *	O	BETA HIFI audio playback output mute signal. Muting when "L".
11	PF3	A INS *	O	Audio insert signal. "H" during audio insert.
12	PC0	NORMAL MUTE *	O	Normal audio playback output mute signal. Muting when "H".
13	PC1	$\overline{\text{VD INT}}$ *	O	Servo reference signal outside/inside switching output. Selects outside reference signal as "H" when recording video signals.
14	PC2	HC CONT	O	CTL head recording current control signal. Normally "L" and "H" when recording video signals.
15	PC3	IND ERA	O	INDEX erase signal. Normally "L". Pulse when erasing INDEX.
16	PD0	IND WRT	O	INDEX write signal. Normally "L". "H" when starting REC. Pulse when writing INDEX in PB mode.
17	PD1	$\overline{\text{CAP RVS}}$	O	Inverting signal of CAP FWD signal input of Pin ㉑.
18	PD2	×1 RVS	O	Not used.
19	PD3	$\overline{\text{TPS}}$	O	Switching signal of capstan control by the SLOW microcomputer or servo IC. "L" during SLOW microcomputer control. "H" during servo IC control.
20	PG0	DRM COMP	O	Reset signal for the digital servo IC (IC006).
21	PG1	$\overline{\text{CP CUT}}$	O	Signal to turn capstan phase servo OFF. This is used to prevent noise position becoming fixed on the screen during variable speed playback. "L" when in CUE/REV/$-\times1$/$-\times2$ modes in β I and in the $-\times1$ mode in β III.

Table 2-6 (1)

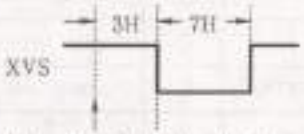
Terminal No.	Port	Signal	I/O	Function
22	PG2	LIM PL S	O	Limiter solenoid start signal. "H" for 200 msec when limiter solenoid activated.
23	PG3	LIM PL H	O	Limiter solenoid hold signal. "H" when FF or REW.
24	PH0	UN BRK PL S	O	Brake solenoid start signal. "H" for 200 msec when brake solenoid activated.
27	PH1	UN BRK PL H	O	Brake solenoid hold signal. "H" when brake released.
28	PH2	PINCH S	O	Pinch solenoid start signal. "H" for 200 msec when pinch solenoid activated.
29	PH3	PINCH H	O	Pinch solenoid hold signal. "H" when pinch roller is operating.
30		XTAL		Clock oscillator terminal. Clock frequency 4.19 MHz.
31		EXTAL		
32	$\overline{RST}$	$\overline{RESET}$		INITIAL RESET signal from the timer microcomputer (IC401 of the TM-92 board). "L" when reset.
33	PX0/$\overline{SC}$	$\overline{SCK}$	O	Serial clock output. Serial communications signals with MECH CON (IC401).
34	PX1/SOB	SO	O	Serial data output.
36	PX3/SI	SI	I	Serial data input.
35	PX2/SOA	H SFT	I	Controls output timing of the XVS signal (Pin ㊾) in the SLOW mode of β II or β III. Normally "L". "H" ... 3H, 7H "L" ... 6H, 1H or 5.5H, 1H (Examle) 3H, 7H  Rise/Fall of RF SW P.
37	PY0	C UNLOAD *	O	Cassette loading motor control signal. "H" when ejecting.
38	PY1/$\overline{PWM}$	C LOAD *	O	Cassette loading motor control signal. "H" when loading.
39	PY2/WP	XVDT	I	Holds output timing of the XVS signal (Pin ㊾) at 6H, 1H or 5.5H, 1H at "H" in the SLOW mode of β II or β III. Switches between 6H 1H and 5.5H 1H when "L". This signal is normally "H".
40	PY3/$\overline{EC}$	CTL	I	VD (REC CTL) signal is input when REC and CTL (PB CTL) signal is input when PB. Signal for SLOW control/INDEX control.
41	PL0	STEP PLS	O	Outputs "H" pulse when driving or stopping the capstan in the SLOW mode.
42	PL1	TEN REG PL *	O	Not used.
43	PL2	DRUM SLOW (WVDK)	O	"H" when XVS (Pin ㊾) is of 6H, 1H or 5.5H, 1H timing. "L" when timing is 3H 7H.
44	PL3	XVE	O	Outputs "L" pulses ("⊔") when XVDT (Pin ㊾) becomes "L" and the SLOWmicrocomputer detects this.

Table 2-6 (2)

<table>
<tr><th>Terminal No.</th><th>Port</th><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>45</td><td>PM0</td><td>XVS</td><td>O</td><td>Pseudo vertical sync signal created from the RF SW pulse. In the digital picture system, memory write of the playback image is executed during variable speed playback with this signal as the timing signal.</td></tr>
<tr><td>46</td><td>PK0</td><td>REEL FG S</td><td>I</td><td>This signal is to calculate remaining tape. The SLOW microcomputer measures the rotating cycle of the S reel with this signal.</td></tr>
<tr><td>47</td><td>PK1</td><td>REEL FG T</td><td>I</td><td>This signal is to calculate remaining tape. The SLOW microcomputer measures the rotating cycle of the T reel with this signal.</td></tr>
<tr><td>48</td><td>PK2/TI</td><td>CAP FG</td><td>I</td><td>Signal for SLOW control. Decides stopping position of the tape (capstan) by the number of CAP FG pulses from startup of the CTL signal (Pin ㊵).</td></tr>
<tr><td>49</td><td>PK3/PM1</td><td>RF SW P</td><td>I</td><td>Signal for SLOW control and generation of XVS.</td></tr>
<tr><td>50</td><td>PI0</td><td>CTL PLS</td><td>O</td><td>Pseudo signal in the event that PB CTL cannot be detected during SLOW control. "H" pulse output.</td></tr>
<tr><td>51</td><td>PI1</td><td>SCE</td><td>O</td><td>Signal that decides whether MODE CON counts PB CTL or pseudo CTL (CTL PLS). "H" when counting pseudo CTL during SLOW/STILL playback.</td></tr>
<tr><td>52</td><td>PI2</td><td>C/R + ×2*</td><td>O</td><td>"H" when in the CUE/REVIEW or ×2 mode.</td></tr>
<tr><td>53</td><td>PI3</td><td>SL TRG</td><td>O</td><td>Trigger output signal of the SLOW tracking control. Normally "L", HIZ (open) for about 100 μsec during SLOW tracking control.</td></tr>
<tr><td>54</td><td>PJ0</td><td>SL TRA</td><td>I</td><td>The SLOW microcomputer measures the time from change of the 1.5 Vdc SL TRA terminal voltage to 3.3 Vdc and changes the stopping position of the capstan (tape) according to this time.</td></tr>
<tr><td>55</td><td>PJ1</td><td>STEP</td><td>I</td><td>Control signal from MECH CON. The SLOW microcomputer executes the following six operations according to the state of CAP FWD (Pin ㊸), SLOW (Pin ㊹) and STILL (communications data from MECH CON at time of startup (¬_) of the STEP signal.
<table>
<tr><th>CAP FWD</th><th>SLOW</th><th>STILL</th><th>Operation</th></tr>
<tr><td>H</td><td>L</td><td>H</td><td>STILL → PB</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>STILL → −×1</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>PB → STILL</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>−×1 → STILL</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>STILL → FWD → STILL</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>STILL → RVS → STILL</td></tr>
</table></td></tr>
<tr><td>56</td><td>PJ2</td><td>SLOW</td><td>I</td><td>Control signal from MECH CON. SLOW operation is decided by the signal level at startup of the STEP signal.</td></tr>
<tr><td>57</td><td>PJ3</td><td>CAP FWD</td><td>I</td><td>Control signal from MECH CON. SLOW operation is decided by the signal level at startup of the STEP signal.</td></tr>
<tr><td>58</td><td>INT</td><td>CAP FG (INT)</td><td>I</td><td>Interrupt occurs for each fall (¬_) of the CAP FG signal.</td></tr>
</table>

Table 2-6 (3)

Terminal No.	Port	Signal	I/O	Function
60	PA0	H SEARCH *	O	"H" during digital scan.
61	PA1	$\overline{\text{SLOW CS}}$	I	Serial communications carried out with MECH CON when SLOW CS is "L".
62	PA2	SKEW IN	I	Not used.
63	PA3	REC *	O	"H" in the REC, REC PAUSE, INSERT and INSERT PAUSE modes.
64	PB0	LINE MUTE *	O	Audio output mute signal. Normally "L". "H" during transition from STOP to PB mode. "H" during variable speed playback.

Table 2-6 (4)

2-4. JOG/SHUTTLE MICROCOMPUTER

The JOG/SHUTTLE microcomputer creates speed signals (SPEED A - C), direction signals (DIRECTION) and pulse signals (ROL PULSE) corresponding to JOG dial rotation or SHUTTLE ring position.

MODE CON reads signals from the JOG / SHUTTLE microcomputer by setting the J/S RQST signal to "L" in each field. These signals are converted to mode commands in the EDIT SEARCH mode and sent to MECH CON. Editing point search is then conducted during assemble editing and insert editing. The SPEED A - SPEED C and Direction signals are used at this time. The ROL PULSE and DIRECTION signals are sent by serial communications from MODE CON to the TIMER microcomputer and also to the CRT microcomputer. These are used for timer / clock settings and for tuning. ROL PULSE also outputs pulses for each click of the JOG dial.

The JOG/SHUTTLE microcomputer also has BETA MODE discrimination functions of the playback tape, DFG (capstan FG) pulses for each CTL signal cycle and this is used for mode discrimination. Discrimination results are transferred to MECH CON (IC401 of SS-80 board) by the two signals of BETA MODE A and BETA MODE B.

2-4-1. JOG/SHUTTLE Microcomputer Port Allocation

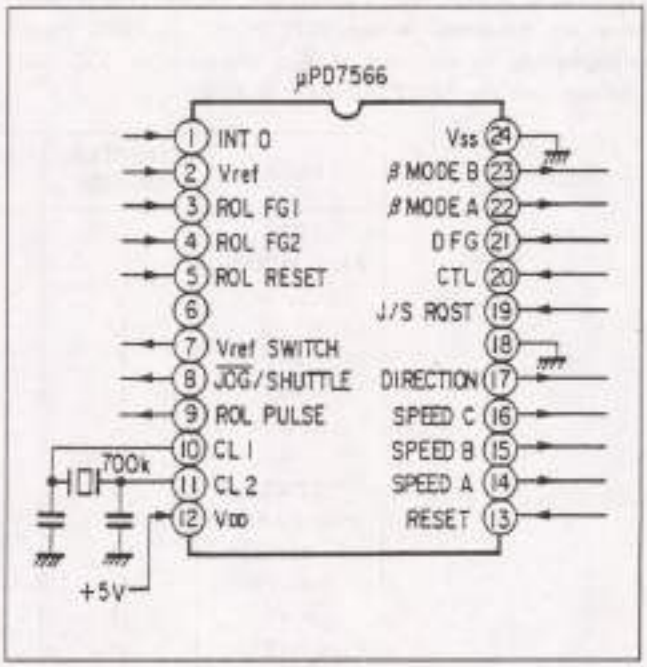


Fig. 2-36

2-4-2. JOG/SHUTTLE Microcomputer Terminal Functions

Port No.	Function	Port No.	Function
1	External interrrupt terminal (Inputs CAP FG)	13	RESET terminal
2	Built-in comparator REF input	14	SPEED mode output (See Table 2-8)
3	JOG dial FG1 input	15	
4	JOG dial FG2 input	16	
5	JOG dial RESET input	17	DIRECTION output
6		18	GND connection
7	Changes over comparator REF voltage	19	Data output request input
8	JOG/SHUTTLE discrimination output	20	CTL input
9	ROL PULSE output	21	DFG (Capstan FG) input
10	CLOCK	22	β mode output (See Table 2-9)
11		23	
12	POWER supply	24	GND

Table 2-7

2-4-3. Logical Mode Table

The operating mode signals (composed of the four signals DIRECTION, SPEED A – SPEED C) shown in the table below are generated in the EDIT POINT SEARCH mode corresponding to the number and direction of JOG dial rotations and the SHUTTLE ring position.

MODE	DIRECTION (Pin ⑪)	SPEED A (Pin ⑭)	SPEED A (Pin ⑮)	SPEED A (Pin ⑯)
STILL	L	L	L	L
FWD FRAME	L	H	L	L
(×1/10)	L	L	H	L
×1/5	L	H	H	L
×1	L	L	L	H
(×2)	L	H	L	H
(×10)	L	L	H	H
—	L	H	H	H
STILL	H	L	L	L
RVS FRAME	H	H	L	L
(−×1/10)	H	L	H	L
−×1/5	H	H	H	L
−×1	H	L	L	H
(−×2)	H	H	L	H
(−×10)	H	L	H	H
—	H	H	H	H

The modes in parentheses are only possible with the SHUTTLE ring.

Table 2-8

2-4-4. Logical BETA Mode Table

Discrimination of the BETA mode is by means of the relation between the CTL input of Pin ⑳ and the DFG of Pin ㉑.

β MODE	β MODE A Pin ㉒	β MODE A Pin ㉓
β I	L	L
β II	L	H
β III	H	L

Table 2-9

2-4-5. Parallel Comunications between the JOG/SHUTTLE Microcomputer and MODE CON

MODE CON sets communication request (J/SRQSR Pin ㉔) to the JOG/SHUTTLE microcomputer to "L" once in each field. The JOG/SHUTTLE microcomputer then outputs the DIRECTION, SPEED A – C JOG/SHUTTLE , and signals. After leaving time for the data to be determined, MODE CON then reads the data and returns the J/S RQST signal to "H" after completing read.

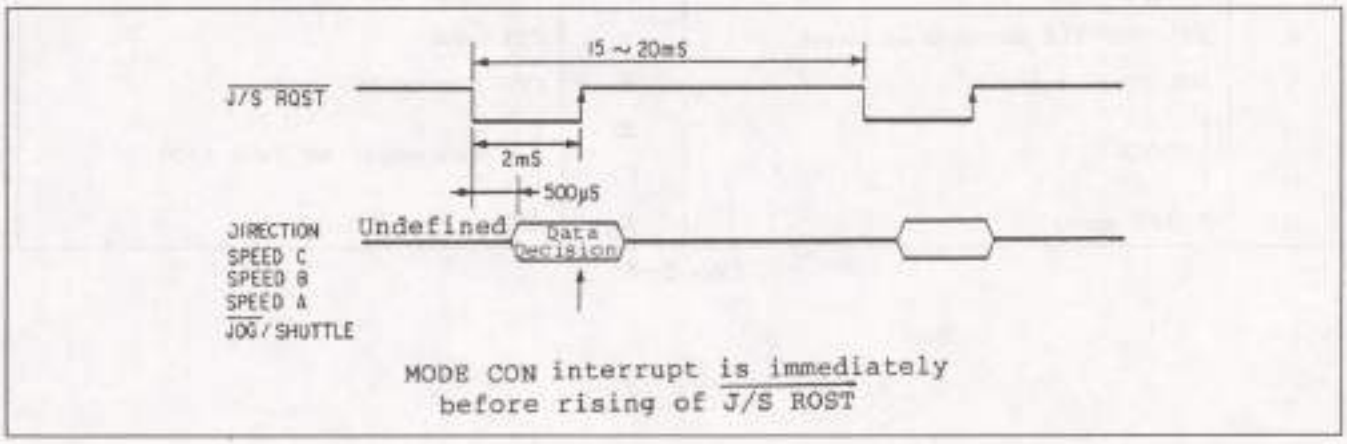


Fig. 2-37

2-5. CRT MICROCOMPUTER AND CHARACTER GENERATOR

Data is provided to character generator IC300 (μPD6142) of Board VE-1 by CRT microcomputer IC402 (CXP5048) of Board TM-92. The CRT microcomputer receives serial data from Timer Microcomputer IC401 and Mode Control IC501 of Board MO-5 and controls the display.

The CRT microcomputer receives data from MODE CON and data from the timer microcomputer by switching over the data with the output of Pin ㊿. Clock from the serial bus is received on Pin ㊾ during communications between these two microcomputers. However, clock is output from Pin ㊾ when sending data to the character generator. In this case, clock output is separated from the bus line by the output signal of Pin ㊿.

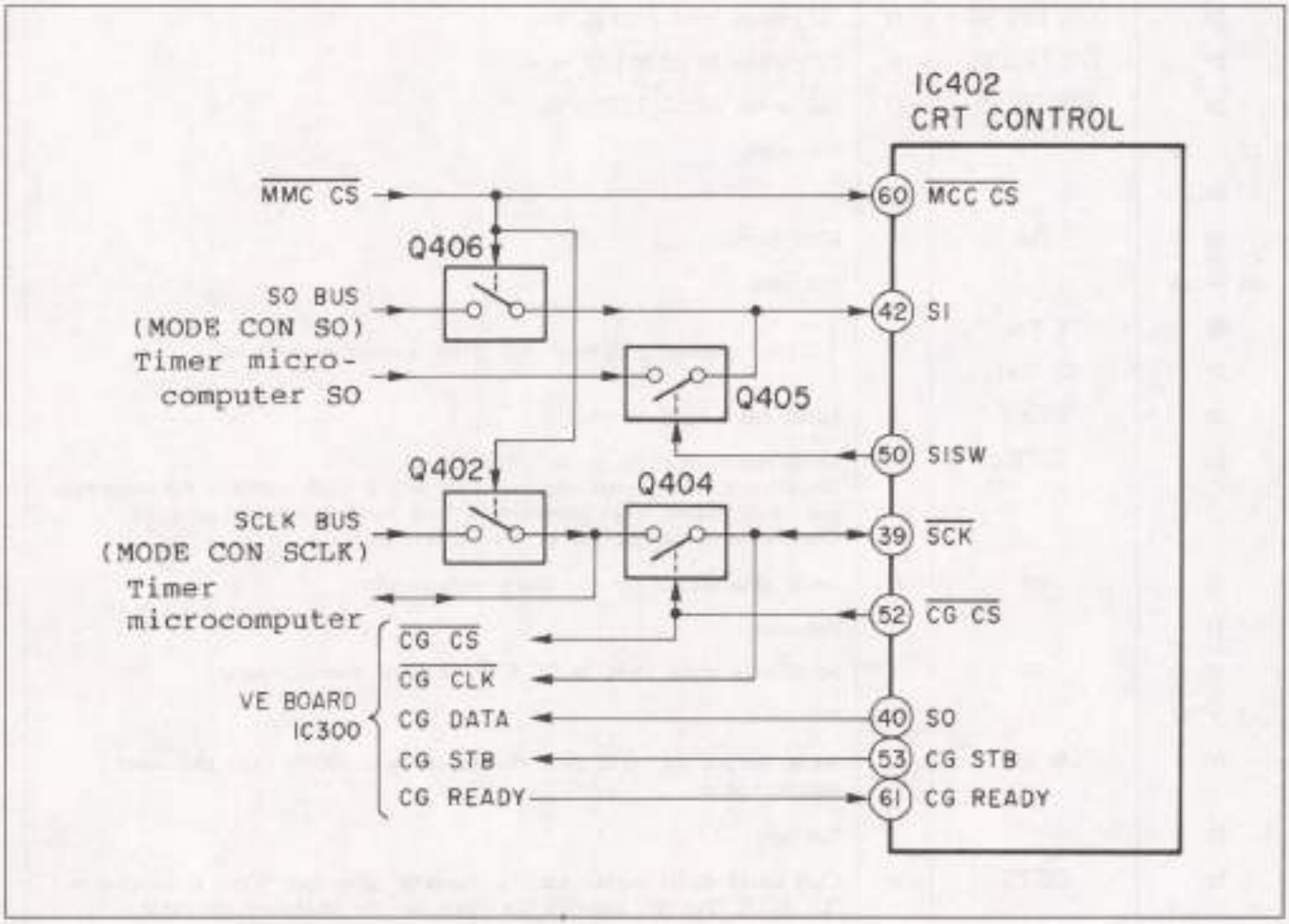


Fig. 2-38 CRT control block diagram

2-5-1. CRT Microcomputer Terminal Functions

Terminal No.	Signal	I/O	Function
1	$\overline{\text{TMCS}}$	I	Tip select signal input. See Table 2-11.
2 - 17			Not used.
18	$\overline{\text{J/S LED F5}}$	O	"L" when CUE LED is lit.
19	$\overline{\text{J/S LED F4}}$	O	"L" when ×2 LED is lit.
20	$\overline{\text{J/S LED F3}}$	O	"L" when ×1 LED is lit.
21	$\overline{\text{J/S LED F2}}$	O	"L" when 1/5 LED is lit.
22	$\overline{\text{J/S LED F1}}$	O	"L" when 1/10 LED is lit.
23	$\overline{\text{J/S LED R1}}$	O	"L" when −1/10 LED is lit.
24	$\overline{\text{J/S LED R2}}$	O	"L" when −1/5 LED is lit.
25	$\overline{\text{J/S LED R3}}$	O	"L" when −×1 LED is lit.
26	$\overline{\text{J/S LED R4}}$	O	"L" when −×2 LED is lit.
27	$\overline{\text{J/S LED R5}}$	O	"L" when REVIEW LED is lit.
28	$\overline{\text{STILL LED}}$	O	"L" when STILL LED is lit.
29 - 30			Not used.
31			
32	Vss		GND terminal
33 - 35			Not used.
36	X TAL		Crystal oscillating element (5.0 MHz) connecting terminal.
37	EX TAL		
38	$\overline{\text{RESET}}$	I	Initial reset input terminal.
39	$\overline{\text{SCLK}}$	I/O	Serial communications clock I/O terminal. Clock input when communicating with MODE CON andtimer microcomputer, and clock output when transmitting data to the character generator. Changeover is carried out by $\overline{\text{CG CS}}$ (Pin ㊷).
40	SO	O	Serial data output for the character generator.
41			Not used.
42	SI	I	Serial data input from MODE CON or timer microcomputer.
43 - 49			Not used.
50	SI SW	O	Signal output for serial data changeover with MODE CON and timer microcomputer.
51			Not used.
52	$\overline{\text{CG CS}}$	O	Chip select signal output for the character generator. When this signal is "L", $\overline{\text{SCLK}}$ (Pin ㊴) becomes the clock for the character generator.
53	CG STB	O	Serial data strobe signal output for the character generator.
54 - 59			Not used.
60	$\overline{\text{MCC CS}}$	I	Tip select signal input. See Table 2-11.
61	CG READY	I	Character generator data output enable signal input and data (Pin ㊶) will not be output to the character generator if "L".
62 - 63			Not used.
64	Vcc		Power supply terminal (+5 V)

Table 2-10

TM CS (Pin ①)	MCC CS (Pin ㉔)	Function
L	L	Received serial data from the timer microcomputer. Data is input to the SI port (Pin ㉒).
H	L	Receives serial data from MODE CON. Data is input to the SI port (Pin ㉒).
×	H	Controls the character generator.

Table 2-11

2-5-2. Function of the Character Generator

The character generator (IC300 of Board VE-1 : μPD6142C-601) generates character signals (Pin ⑨ : Outputs from terminal V_R) synchronized with signals $\overline{VD}$ and $\overline{HD}$ separated from the video signal based on data received by serial communications from the CRT microcomputer.

Data such as "character background" (2 types), "character size" (4 types), "row address", "column address", "character data" (64 types), and "display ON/OFF" are transferred in serial communications. Furthermore, the length of all data is eight bits and one data is transferred for each communication.

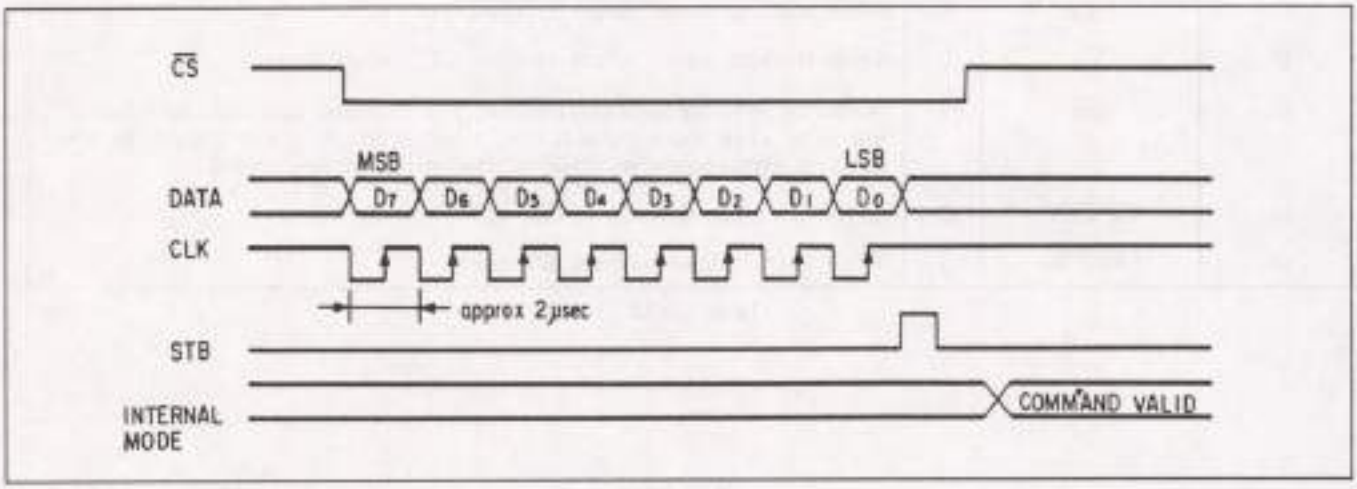


Fig. 2-39

2-5-3. Character Generator Terminal Functions

Terminal No.	Signal	I/O	Function
1	DATA	I	Input terminal for the serial data from the CRT microcomputer (IC402 of Board TM-92). Read by synchronizing with the clock signal input from the CLK terminal.
2	CLK	I	Data read clock input terminal. Data is read with rise of the clock signal.
3	STB	I	Strobe signal input terminal. Eject bit data read with rise of the strobe signal. If the eight bit data is a character data ($D_8 = 0$, $D_7 = 0$), data address increases with fall of the strobe signal.
4	$\overline{CS}$	I	Chip select signal input terminal. "L" during serial data input.
5	V_{DD}	O	+5 V power supply
6	OSC OUT	O	Oscillation terminal. Connected to L and C.
7	OSC IN	O	
8	V_{SS}	O	GND terminal
9	V_R	O	Character data output terminal. "H" when active. Only VR terminal used.
11	V_G	O	
12	V_B	O	
10	V_{BLK}	O	Video blanking signal output terminal. "H" when active.
13	$\overline{VD}$	I	Video blanking signal output terminal. "L" when active.
14	$\overline{HD}$	I	Horizontal sync signal input terminal. The character generator oscillates internally when the horizontal sync signal is at "H" level. Oscillation also starts in synchronism with rise of the horizontal sync signal.
15	$\overline{CK\ OUT}$	O	Inversion output terminal of $\overline{OSC\ OUT}$ (Pin 6), Not used.
16	$\overline{TEST\ IN}$	I	TEST CLOCK input terminal. Not used.

Table 2-12

2-6. CONTROL T TERMINAL

2-6-1. Basic Configuration

High accuracy editing is possible by using two of these units in a preroll system. To realize this system, it will be necessary to control the mating unit while checking its state. The use of Control L may therefore be coinsidered for this purpose.

Control L is the signal connecting the primary controller and the controlled controller.

This signal is to connect an editing controller or wired remote controller and a VTR, and to control the VTR by out putting commands from the controller while observing VTR information (counter value, mode, etc.). In other words, VTRs cannot be mutually connected with control L. VTRs are therefore mutually connected by providing a separate circuit to output commands to the primary VTR and connecting this to control L of the mating VTR. When editing with two VTRs, the general practice is for one-way connection of the audio and video signals. That is, use is limited to playback for one and recording for the other. Editing is broadly divided into assemble editing and insert editing. In the former, editing isexpedited with the playback-side having control rights and, in the latter, if the recording side has control rights. In the case of the control signals, it will therefore be necessary to connect the mutual control L input and output in crossed form.

Since using two cables for this purpose will be wasteful and connection will become complicated, the two I/O signals are combined into one in control T and a stereo minijack used. VK-1000T with the cables crossconnected inside is used for this purpose.

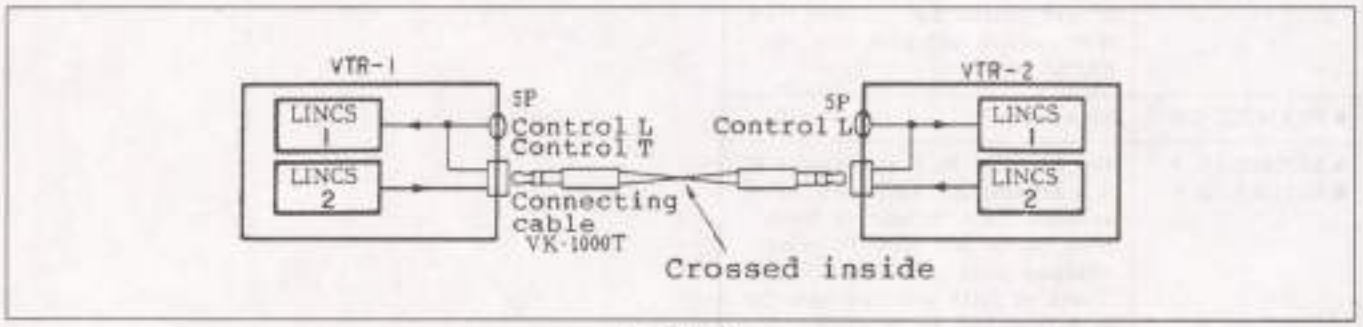


Fig. 2-40

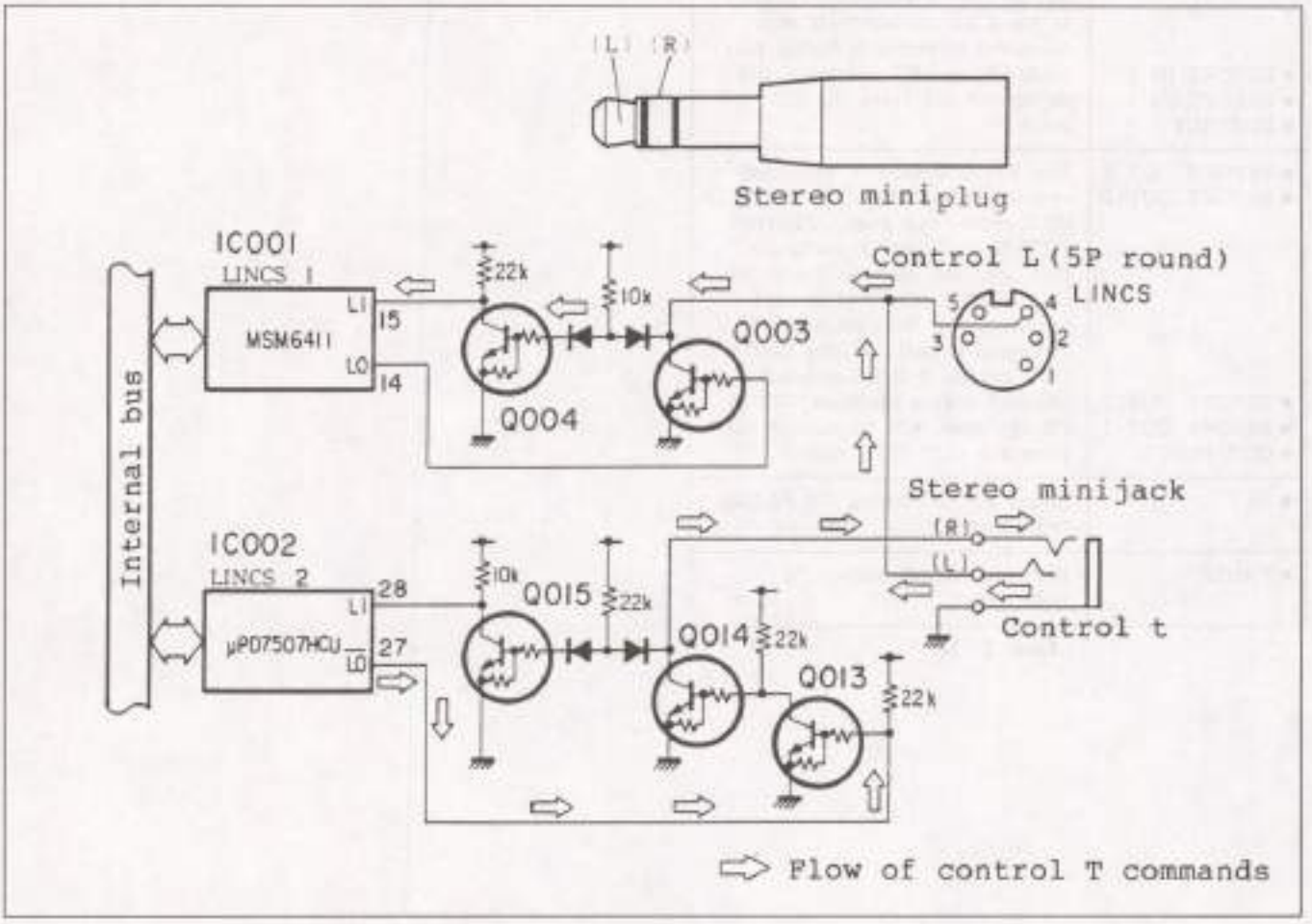


Fig. 2-41

2-6-2. Circuit and Operation

A stereo minijack is the control T terminal of the main VTR unit and the No. ④ pin of the conventional control L terminal (5P round) is connected to the L ch. The output signal of the LINCS 2 microcomputer is connected to the R ch. The circuit is as shown in Fig. 2-46 with a standard LINCS circuit used as the external interface.

The commands output from LINCS 2 to the other VTR and the operation of the VTR receiving these commands are as shown below.

Command	Operation of the VTR receiving the command
• EDIT STANDBY	If received during PB PAUSE, it returns exactly five seconds from that position and goes into PB PAUSE mode.
• FRAMING ON	No action.
• BEFORE IN F • BEFORE IN E ⋮ • BEFORE IN 2 • BEFORE IN 1 • IN POINT	The BEFORE IN F command ("F" is a hexadecimal equivalent to decimal "15") is sent 15 fields prior to the edit CUT IN point (starting point). BEFORE IN E, D, C and so forth are then sent for each field, and an IN POINT command is sent following the BEFORE IN 1 command (exactly at the CUT IN point). If this command is received during playback, PB → REC operation will be carried out from the CUT IN point.
• BEFORE OUT F • BEFORE OUT E ⋮ • BEFORE OUT 2 • BEFORE OUT 1 • OUT POINT	The BEFORE OUT F command is sent 15 fields before the edit CUT OUT point (end point). BEFORE OUT E, D, C and so forth are then sent for each field and an OUT POINT command is sent following the BEFORE OUT 1 command (exactly at the CUT OUT point). If this command is received during playback, REC → PB operation will be carried out from the CUT OUT point.
• PB	Clears PAUSE during PB PAUSE (edit starts).
• PAUSE	Becomes PAUSE during PB (edit ends).

Table 2-13

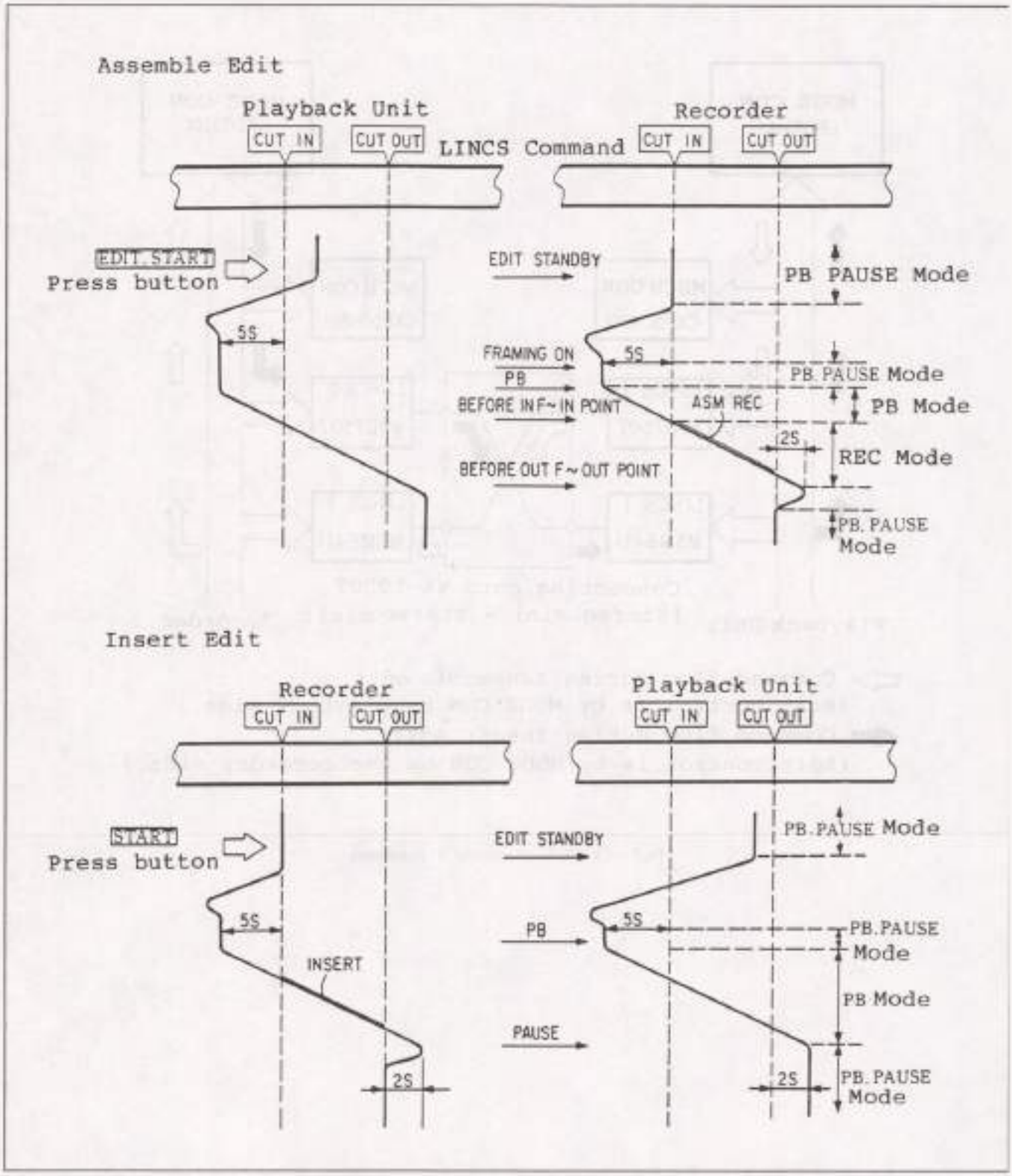


Fig. 2-42 LINCS command transmission timing during preroll editing

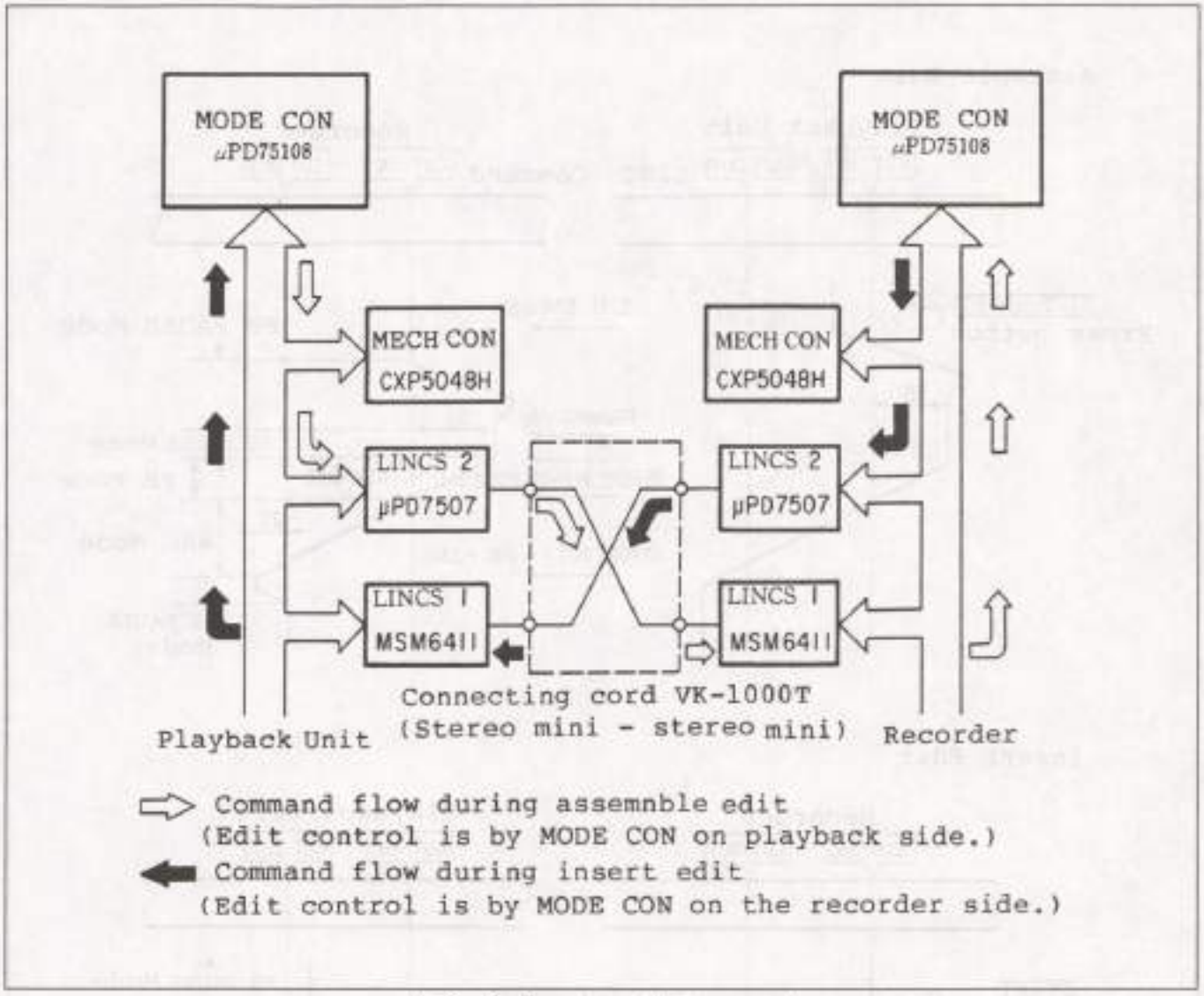


Fig2-43 Flow of control T command

3. SERVO CIRCUIT

3-1. SERVO BLOCK DIAGRAM

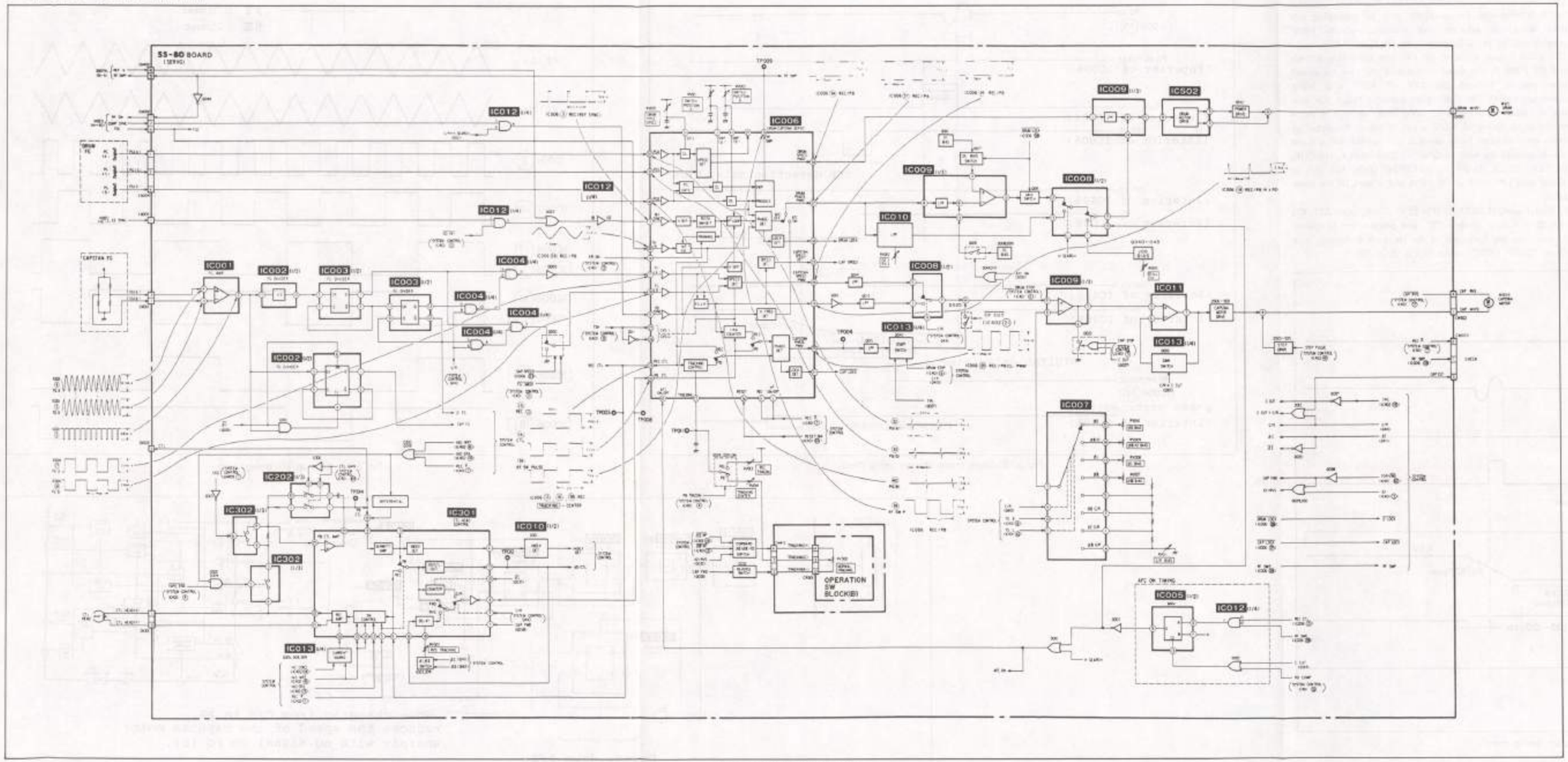


Fig. 3-1 Servo block diagram

3-2. DRUM SERVO

The drum servo is configured of the speed system to control rotating speed and the phase system to control rotation phase.

The phase system servo applies servo by using the signals shown in Table 3-1.

Mode	Control signal	Comparison signal
REC	PG (B)	VD
PB	PG (B)	INT VD

Table 3-1 Phase system servo

When recording, the PG (B) signal and the VD (Vertical Drive) signal separated from the video signal input are phase-compared ; and when playing back, PG (B) and the 3.58 MHz frequency divided INT. VD are compared and the results are output from Pin ㉑ of IC006 as PWM.

The speed system servo uses PG (A) and PG (S) signals for both recording and playback, and by measuring the time difference between the signals, outputs PWM proportional to the difference from Pin ㊳ of IC006.

The IC006 output is called DP PWM in the phase system and DS PWM in the speed system and the two are mixed after passing through the LPF of IC009 and being converted to DC. The signal then passes through the amp and is output from Pin ㉙ of IC009 after which it is input to the drum driver of IC602 where it drives the drum as drum error voltage. Phase servo is not applied and a fixed bias is selected for each by Q040 ~ Q043 when in the CUE, REVIEW, STILL, SLOW or REVERSE mode and this is mixed with LPF OUT of DS PWM and is sent to the drum driver.

In digital scan, H SEARCH (Pin ⑪ of IC008) and AFC ON (Pin ⑯ of IC006) become "H" and phase servo is applied by detecting the frequency of the playback horizontal sync signal (COMP SYNC) input of Pin ⑧ of IC006.

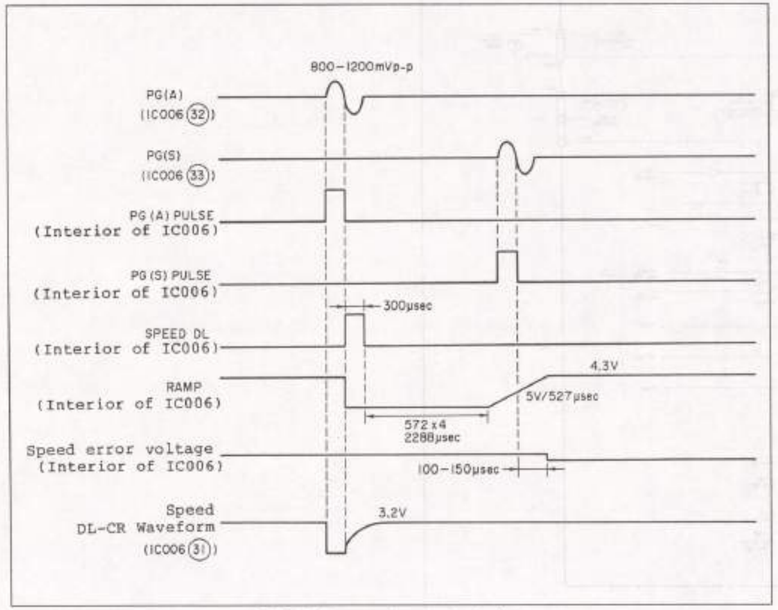


Fig. 3-2 Drum speed system timing chart

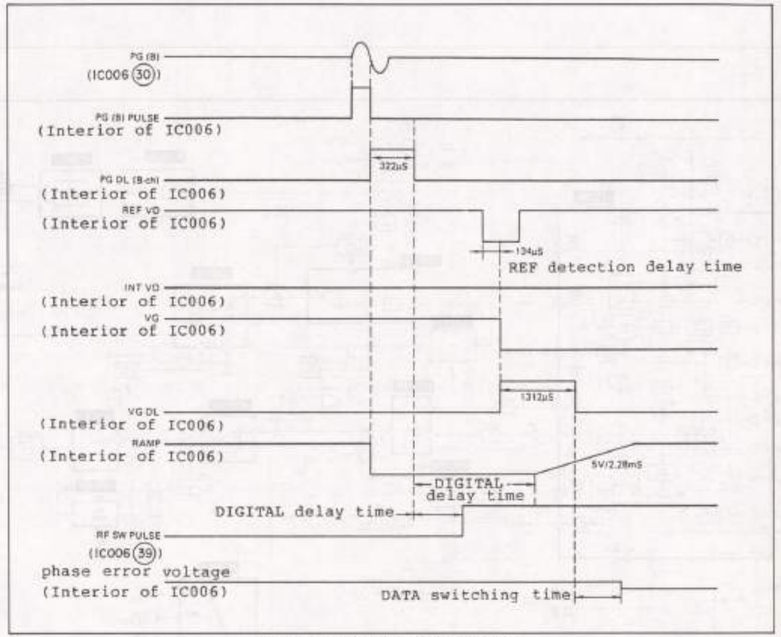


Fig. 3-3 Drum phase system timing chart

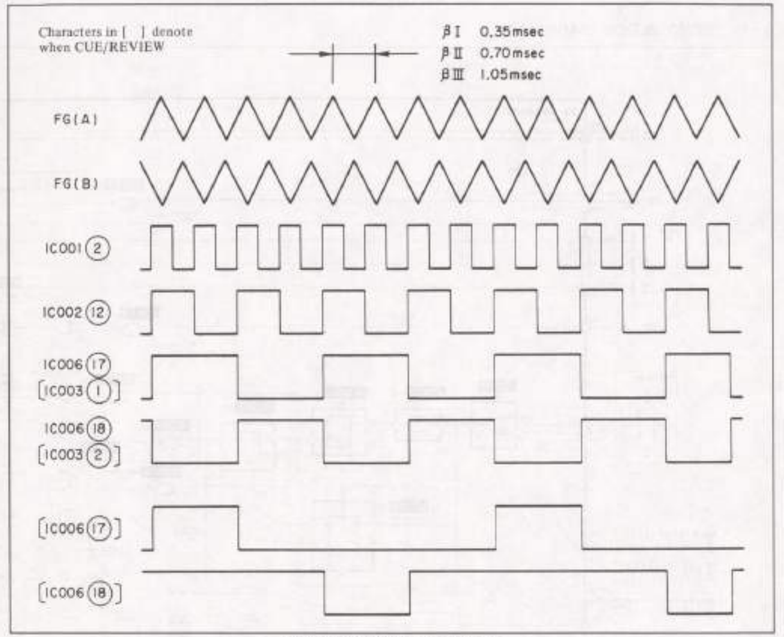


Fig. 3-4 Capstan FG timing chart

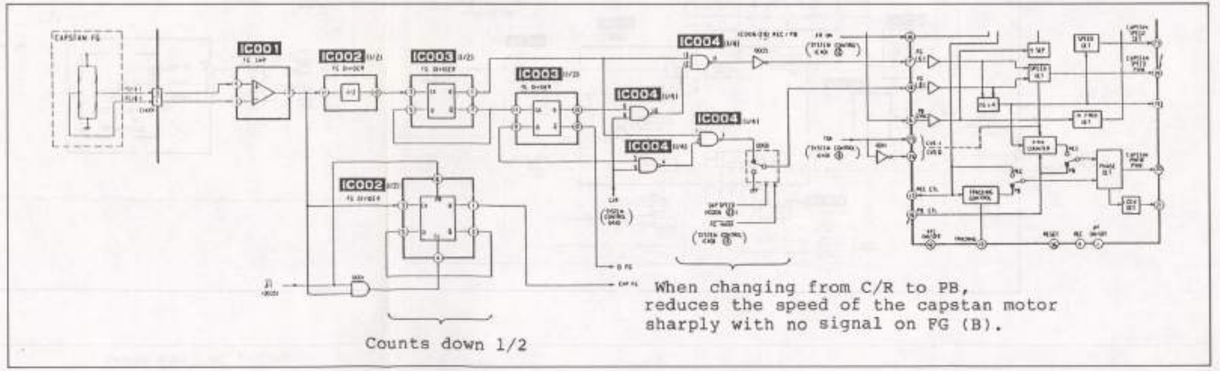


Fig. 3-5 Capstan FG signal processing circuit

3-3. CAPASTAN SERVO

Similar to the drum, the speed system and phase system servo controls are also applied to the capstan.

Mode	Control signal	Comparison signal
REC	Capstan FG 30 Hz	VD
PB	PG (B)	INT VD

Table 3-2 Capstan phase servo

The FG signal has been changed from the conventional 90 pulses per rotation (SL-HF1000, etc.) to 720 pulses per rotation. In line with this, the FG signals that were input to the servo IC with its frequency doubled is now conversely input in this unit after 1/4 frequency division. The higher FG frequency not only improved stability of travel but has also eliminated the need for a switcing circuit for forward and reverse travel as previously required.

Furthermore, in CUE/REVIEW, the FG signal is input to the servo IC after further 1/2 frequency division.

The speed system servo measures the falling time of FG (A) and FG (B) input to Pins ⑰ and ⑱ of IC006 and outputs error as CS PWM from Pin ㉓.

The phase system servo counts down the VD and FG signal and compares this with a 30 Hz signal when recording, and during playback, it compares the CTL signal with TRACON MMV generated in IC006 by synchronizing with INT VD and outputs the error from Pin ㉑ as CP PWM.

In C/R, ×4FG of Pin ⑬ is used to apply servo since sufficient voltage cannot be obtained with CSPWM.

These PWM signals (×4FG is a pulse signal) are mixed after DC conversion in the respective LPF and is compared with the DC bias from IC007 and amplified by IC009. Phase compensation is then carried out in IC011 and the signal is sent to the motor driver to drive the capstan motor.

Capstan servo system timing charts are shown in figures.

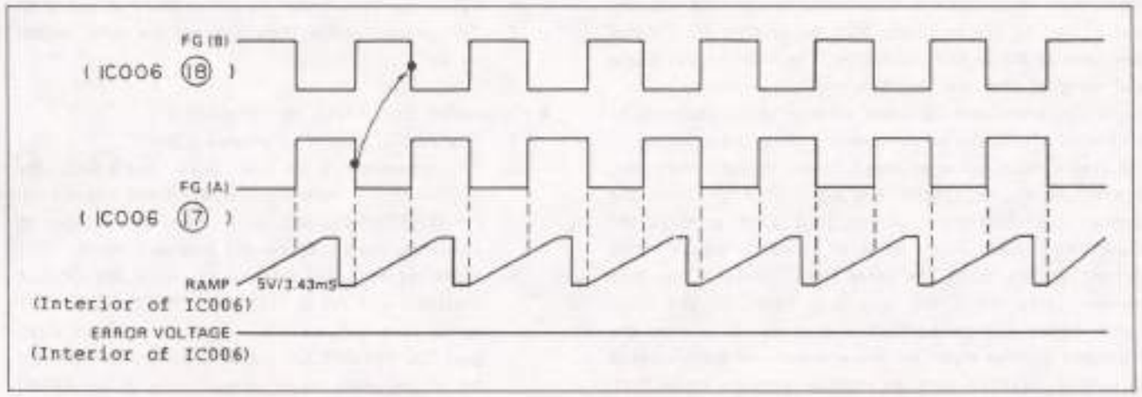


Fig. 3-6 Capstan speed system timing chart

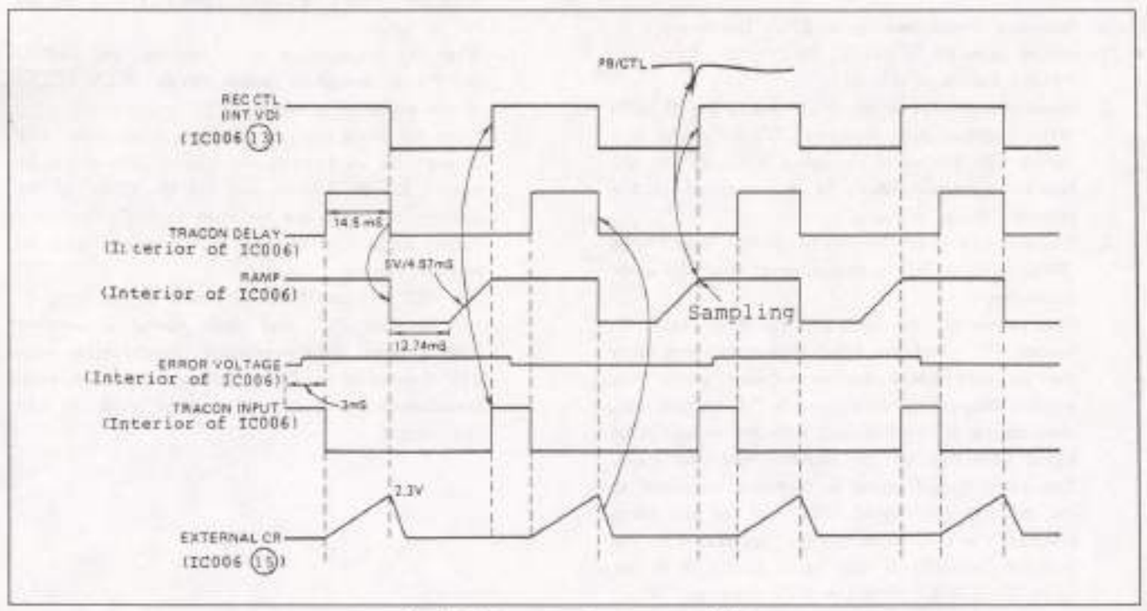


Fig. 3-7 Capstan phase system (PB)

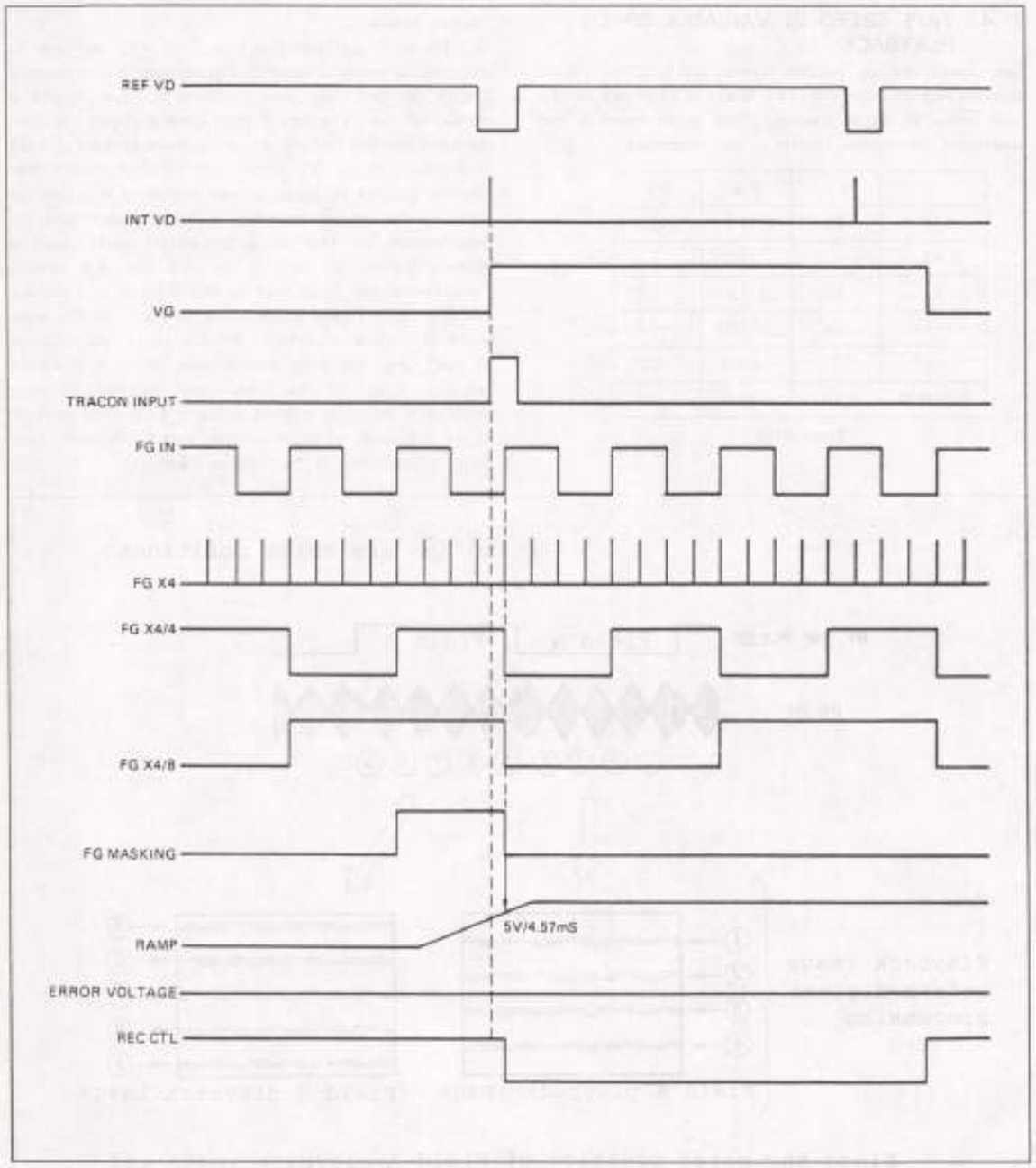


Fig. 3-8 Capstan phase system (REC)

3-4. TAPE SPEED IN VARIABLE SPEED PLAYBACK

Tape speed during variable speed playback to realize noiseless reproduction with two heads is as shown in the table below. In digital scanning, fixed speed travel is not used since the capstan system is not concerned.

	β I	β II	β III
CUE	5.5	10.0	10.0
×2		2.0	2.0
×1	1.0	1.0	1.0
−×1	−1.47	−1.33	−1.0
−×2		−2.0	−2.0
REVIEW	−5.5	−10.0	−10.0

Table 3-3

(Picture Search)

In odd speed multiples (such as ×7, ×9) as used in conventional models, noiseless reproduction is not possible due to the fact that noise positions of Fields A and B overlap on the TV screen. If even speed multiples are used, the noise position of Field A and the noise position of Field B alternate on the TV screen and noiseless reproduction becomes possible by digital pictuer processing in which the signal of the one previous field is used to supplement the noise section. For this reason, the picture search speed is made 10 times as fast in the β II and β II modes. Furthermore, the video head in this machine is made for the β II mode (track width about 29 μm) so the head width is narrow in relation to β I (track width about 58 μm) and the noise bar is wide. Noise is therefore generated even in with even speed multiples. Noiseless playback is therefore realized by using a 5.5 speed multiple in the β I mode so noise position does not become fixed. (−×1 (Monospeed in the Reverse Direction))

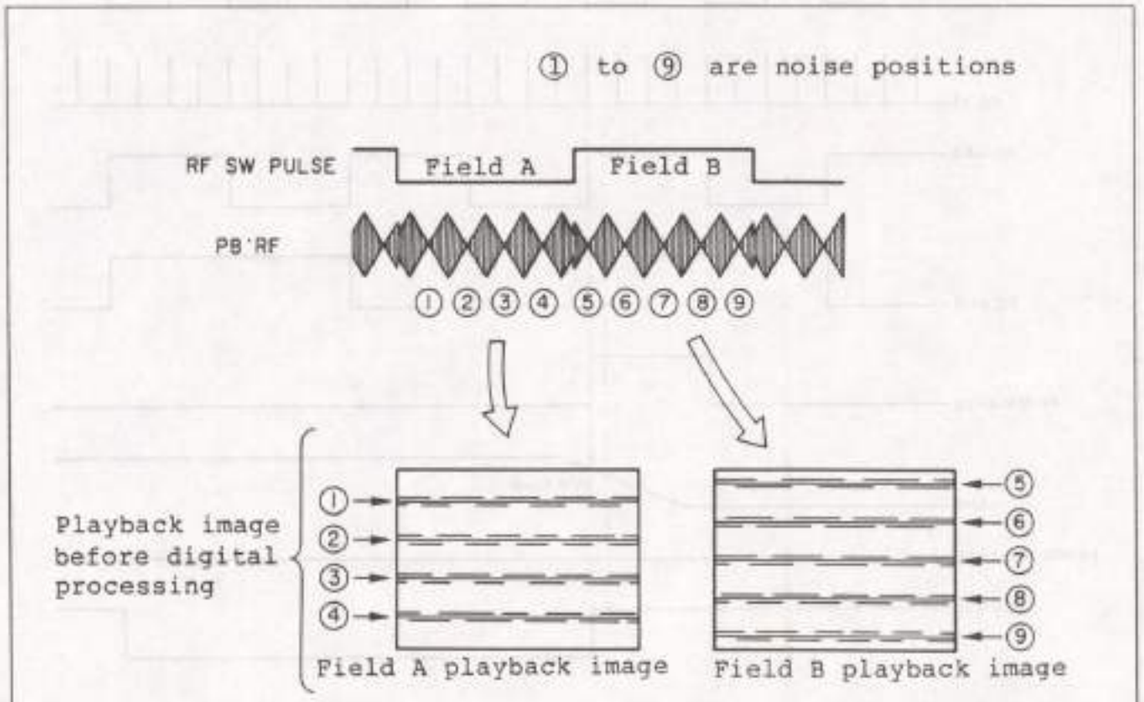


Fig. 3-9 Picture search (×10 Cue) noise position

If accurate monospeed playback is carried out in the reverse direction, the noise bar becomes fixed in the same position on the screen in both the A and B fields and noiseless operation will not be possible. Tape speed is therefore made about 1.4 speed so the noise position does not become fixed.

In the case of the β III mode, noise is not generated even with an accurate monospeed tape feed since the video head is wide in relation to the track width.

3-5. SERVO REFERENCE SIGNAL IN VARIABLE SPEED PLAYBACK

The AFC ON signal of Pin ㊷ of IC006 becomes "H" during variable speed playback (excluding monospeed and double speed) and the drum pahse system operates so the horizontal frequency of the playback sync signal input of Pin ⑥ is of the same value as during normal playback. The reproduced video signal is first stored in the field memory and is read by synchronizing with the synchronizing signal generated in the memory controller. The video output signal and servo system are therefore not in synchrony.

Therefore, when shifting from variable speed playback to normal playback, the servo system is first phase locked to the synchronous signal generated by the memory controller. In other words, the synchronous signal (REF V) from the memory controller input of Pin ③ of IC006 operates the drum and capstan servo as servo reference signals when shifting to this mode. The video signal stored in the field memory (naturally a still image) is output as the video signal during this period. REF V becomes "L" when the drum and capstan servo are phase locked and servo returns to normal operation with the internal reference signal (INT VD) as the reference.

(Servo Reference Signal Switcing in STILL Operation)

- Transition from PB to STILL (PB PAUSE) Mode
  1. PAUSE button is pressed
  2. Memory controller (IC501 of DI board) Pin ㊼ (WE: Write Enable signal) becomes "H" for a one field period with the mode controller (IC501 of the MO board) command. Write is then enabled to the playback image memory.
  3. The memory controller Pin ㊽ (SWM) and Pin ㊾ (RVS) become "H" with commands from the mode controller.
     This causes memory controller Pin ㊻ (SWMM) to become "L" and the video output switches from the playback image to the memory image just written. Because the RVS signal is "H" at this time, read timing is synchronized with the synchronous signal generated by the memory controller itself. The video output signal is therefore unrelated to the internal sync signal (INT VD) of the servo system). The sync signal (REF V) generated by the memory controller is also input to Pin ③ of the servo IC (IC006) while the RVS signal is "H".
  4. With commands from the mode controller, the SLOW/INDEX controller (IC402 of the SS board) sets Pin ⑩ (TPS) to "L". This causes the CAP CUT signal (Pin ⑦ of CN003 of the SS board) to become "H" and the capstan servo goes OFF. The AFC ON signal (Pin ㊷ of IC006) also becomes "H" and the phase servo of the drum servo system switches to a control method in which the Playback fH (COMP SYNC) frequency is fixed.
  5. The SLOW/INDEX controller sets Pin ⑪ (CAP RVS) to "L" and brakes and stops the capstan by outputting PWM waves from Pin ⑪ (STEP PULSE). Capstan movement is detected by the CAP FG signal.
  6. After the capstan stops, memory controller Pin ㊼ (WE) is set to "L" for a one field period by commands from the mode controller and write of STILL playback image to the memory is executed.
  7. This memory image then becomes the video output signal.

- Transition from STILL to PB mode
  1. The PAUSE button is pressed again.
  2. By commands from the mode controller, the SLOW/INDEX controller outputs PWM waves from Pin ⑪ (STEP PULSE) and causes the capstan to accelerate rapidly to normal playback speed.
  3. When capstan acceleration ends, the SLOW/INDEX controller sets Pin ⑩ (TPS) to "H". The CAP CUT signal then becomes "L" and the capstan servo goes ON. The AFC ON signal also becomes "L" and the drum phase error output (Pin ㊺ of IC006) becomes the phase error of the sync signal (REF V) from the memory controller input of Pin ③ and the PG (B) signal.
  4. When the drum phase servo operates and REF V and PG (B) are phase locked, Pin ㊿ (DRUM LOCK) of the servo IC becomes "L".
  5. When the mode controller detects drum phase lock through the mechanism controller (IC401 of the SS board), Pin ㊽ (SWM) and Pin ㊾ (RVS) of the memory controller are returned to "L". The video output signal then switches from memory image to playback image.
     The REF V signal input of Pin ③ of the servo IC also becomes "L" and servo operation switches from external synchronization (synchronizes with REF V input of Pin ③) to internal synchronization (synchronizes with INT VD created from the 3.58 MHz clock).

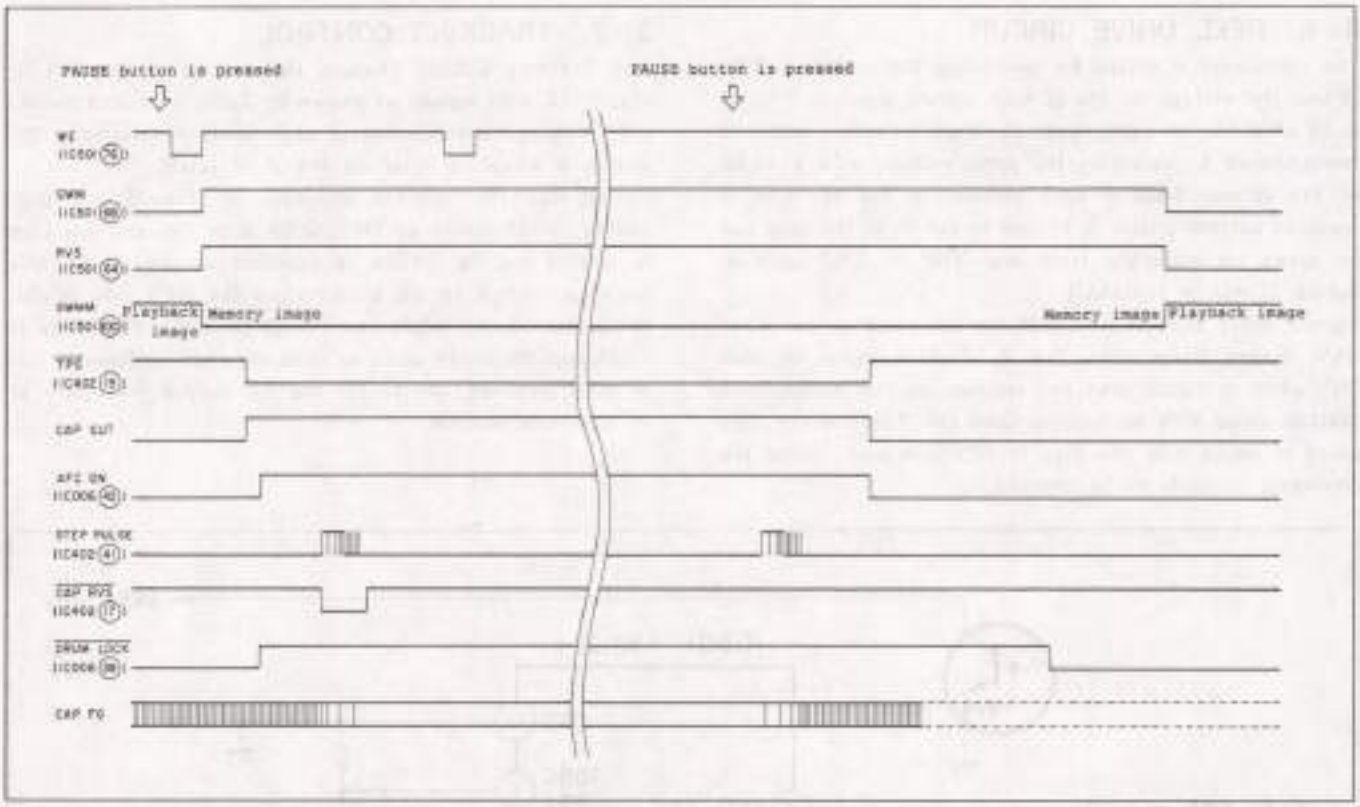

PAUSE button is pressed
PAUSE button is pressed
WE
DWN
RVS
playback image
Memory image
Memory image
Playback image
TPE
CAP OUT
AFC ON
STEP PULSE
CAP RVS
DRUM LOCK
CAP FG

Fig. 3-10

3-6. REEL DRIVE CIRCUIT

The reel motor is driven by controlling the current on Pin ⑮ and the voltage on Pin ⑯ with signals input to Pins ① to ⑪ of IC601 in each mode. Constant voltage control is accomplished by detecting the drive voltage with V SENS of Pin ⑬ and feeding back voltage to Pin ⑭. Also, a constant current circuit is formed in the IC so the tape can be taken up smoothly from any TOP – END position during LOAD or UNLOAD.

Signals other than H SEARCH are the same as for FF/REW during digital scan. The H SEARCH signal becomes "H" when in digital scan and reduces the reel motor drive voltage about 20% by turning Q509 ON. This reduces tape speed to about 20% less than in FF/REW and enables the recording contents to be checked.

3-7. TRACKING CONTROL

The Tracking Control changes the voltage at point A of Fig. 3-12 with signals as shown in Table 3-4 and carries out tracking corresponding to each mode by changing the sawtooth waveform duty on Pin ⑮ of IC006.

During REC, PB TRACON becomes "L". Pins ③ and ④ of analog switch IC014 go OFF, Q028 goes ON and tracking is carried out by RV013. In addition to control by this tracking control circuit, tracking on the RVS side is also controlled by the voltage on Pin ⑱ of IC301. The latter is to change the servo point of drift of track inclination due to RVS playback and to fix the RF output waveform at its optimum position.

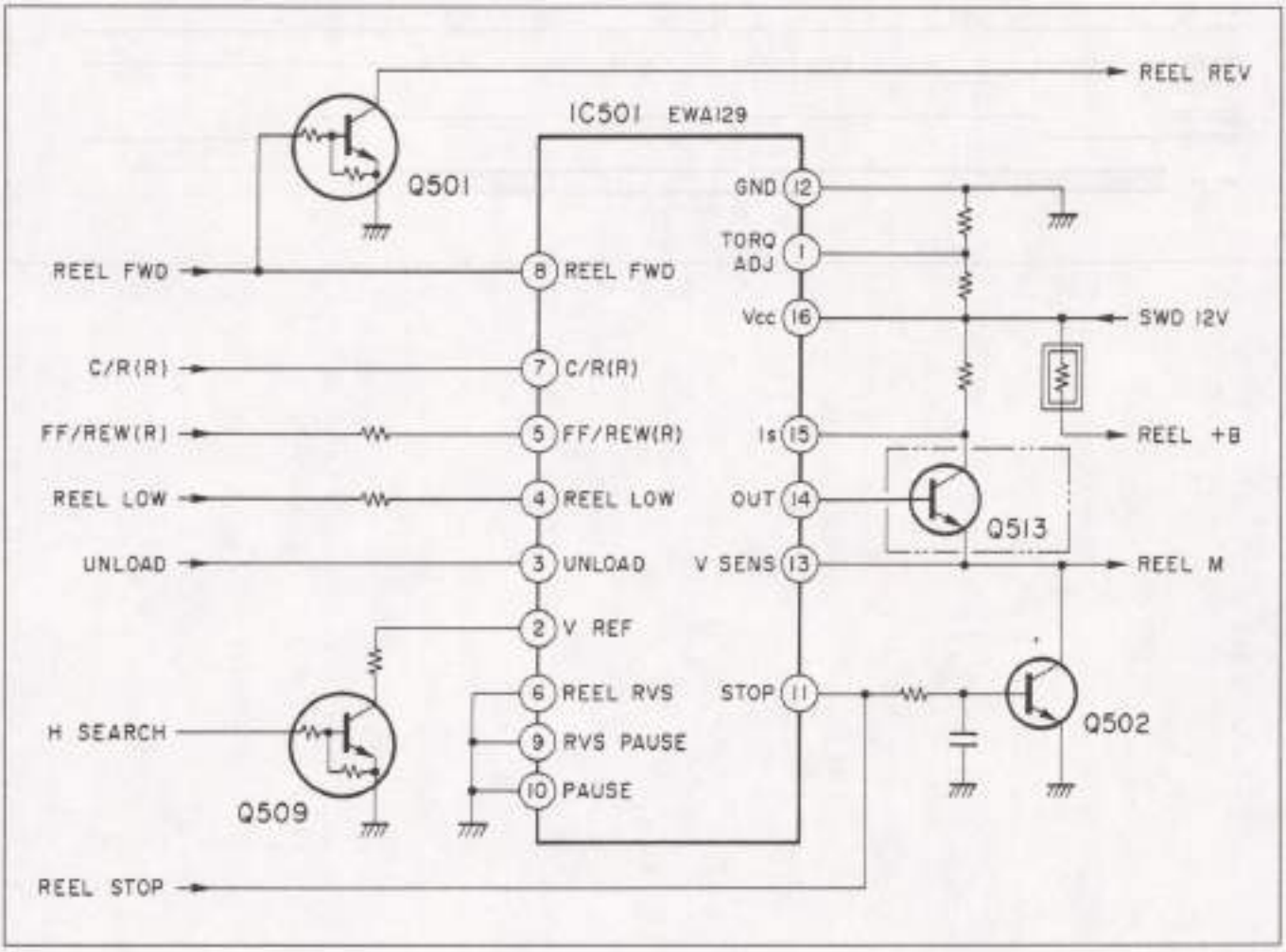


Fig. 3-11 Reel drive circuit

When PB :

Mode / Signal	FWD × 1	FWD × 2	RVS × 1	RVS × 2
PB TRACON	H	H	H	H
$\overline{TOP}$/END	H	H	L	L
β III NP	H (Only when β III)	H (Only when β III)	L	L
β II NP	H (Only when β II)	H (Only when β II)	L	L
FWD$\overline{X2}$	H	L	L	L

Note : PB TRACON "L" in REC.

Table 3-4

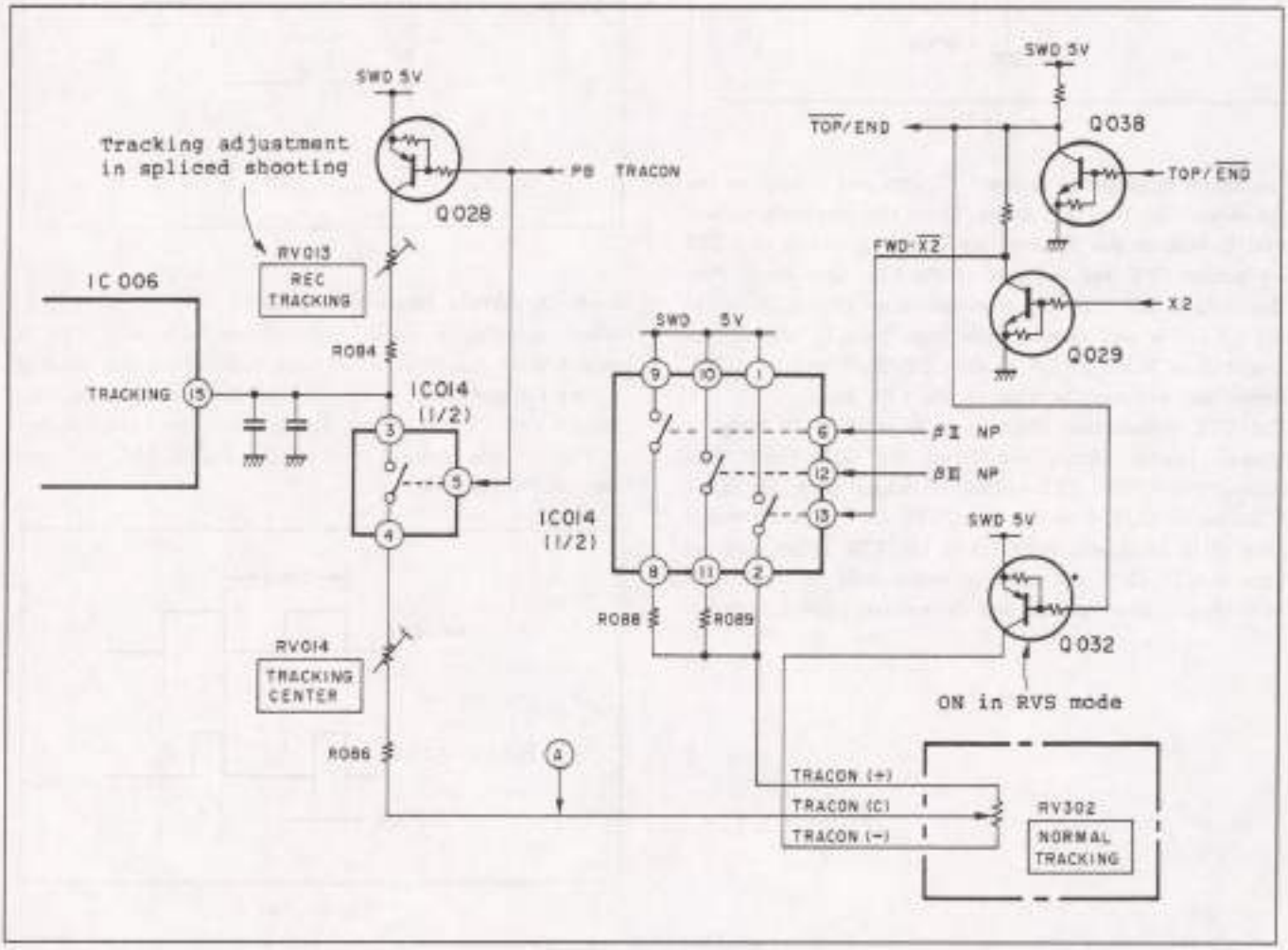


Fig. 3-12 Tracking control circuit

3-8. CTL CIRCUIT

3-8-1. When Playback

The circuit diagram of CTL is shown in Fig. 3-13. Pins ㉑ and ㉒ are as shown in Fig. 3-13 in IC301 during playback. The CTL signals picked up by the CTL head are sent to the CTL amp (Pins ㉑ - ㉓ of IC301).

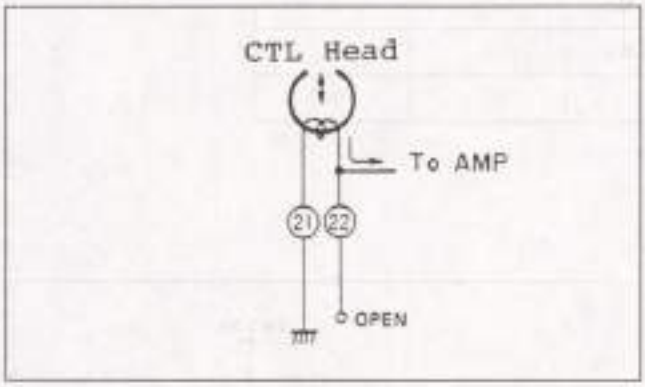


Fig. 3-13

The signal is amplified in the CTL amp and is sent to the comparator in the next stage. Since the playback output level is high in the ED Beta mode, Pins ⑩ and ⑨ of IC302 are turned OFF and the gain of the CTL amp drops. Pins ⑩ and ⑪ of IC302 go ON in modes other than CUE/REV, and FF/REW and remove noise from the CTL signal. Pins ① and ② of IC302 go ON in the CUE/REV and FF/REW modes and reduces the gain of the CTL amp.

The CTL comparator (Pins ① - ③ of IC301) forms a Schmitt trigger circuit and forms the CTL signal into square waves. The CTL output is output from Pin ④ of IC301 as ID OUT, from Pin ⑧ as CTL OUT in an inverted form of ID OUT, and from Pin ⑬ VD/CTL in an inverted form of CTL OUT and are sent respectively to the INDEX DET circuit, servo circuit and system component system.

3-8-2. When Recording

The internal connections of Pin ㉑ and Pin ㉒ of IC301 becomes of equivalent form as shown in Fig. 3-14 when the REC-P signal becomes "H". The current source here is the current that flows into HC of Pin ㉔ of IC301 when HC CONT becomes "H" and turns Q308 ON.

The four switches are synchronized with REC CTL and go ON-OFF in combinations of A-A', B-B' as shown in the diagram, changes the direction of flow of the current in the CTL head, and records CTL on the tape.

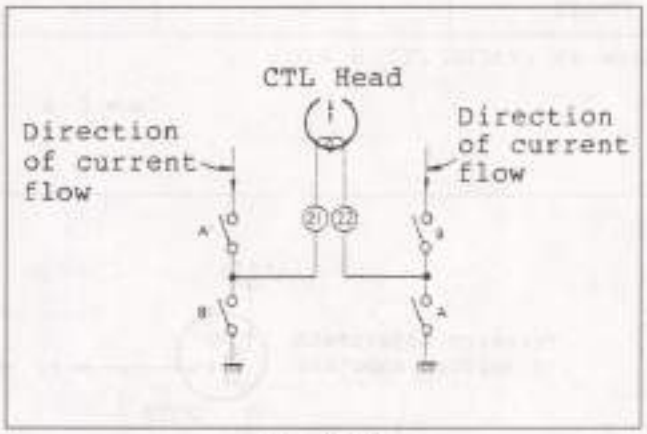


Fig. 3-14

3-8-3. When Recording Starts

When recording, a signal synchronized with REC CTL is output from Pin ⑮ of IC301 and, after waveform shaping by the CR connected to Pins ㉘ and ㉙, creates a 20% duty INDEX REC CTL. When recording starts, the switch shown in Fig. 3-14 is changed over by this INDEX REC CTL and records INDEX CTL.

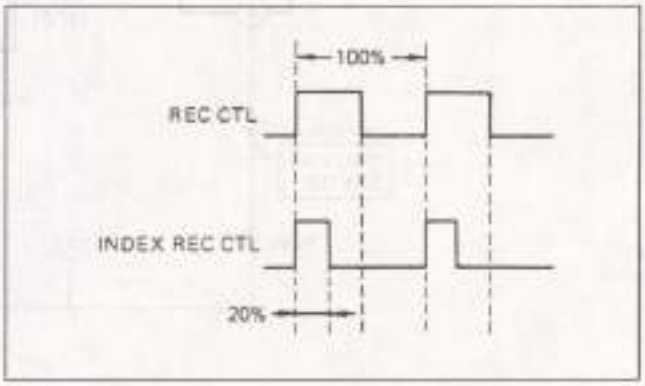


Fig. 3-15

3-8-4. RECORD WRITE

If the INDEX MARK switch is pressed during RECORD WRITE, both INDEX WR and HC CONT signals rise from the point at which the initial CTL falls as counted from the point at which the switch was pressed, and operations same as when recording starts are then carried out.

3-8-5. Playback WRITE

If the INDEX MARK switch is pressed during playback, IND WR and HC CONT signals are output from falling of the initial CTL with the timing shown in Fig. 3-16. The internal connections of Pin ㉑ and Pin ㉒ of IC501 are as shown in Fig. 3-17. The current source here is the current flowing in Pin ㉑.

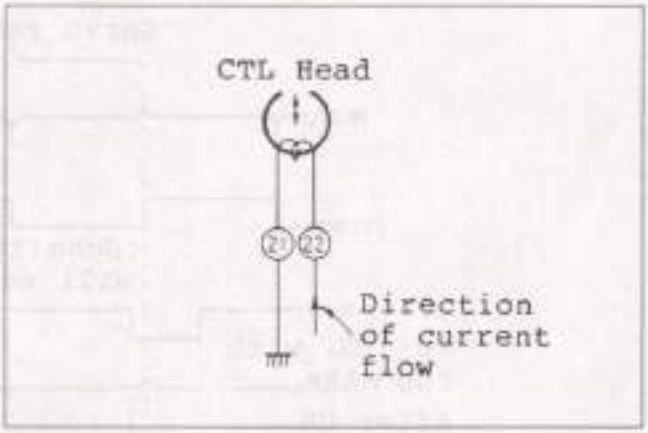


Fig. 3-17

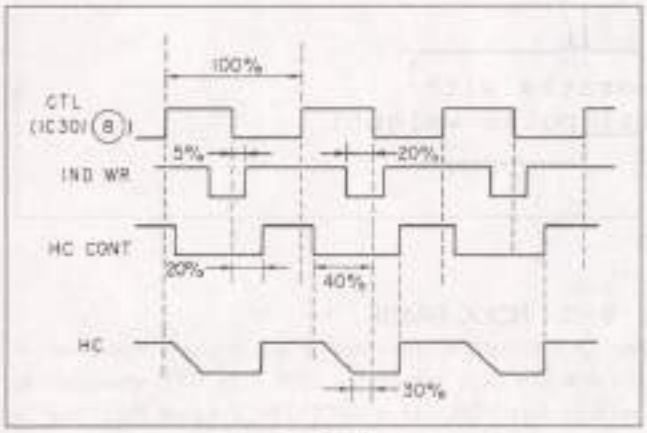


Fig. 3-16

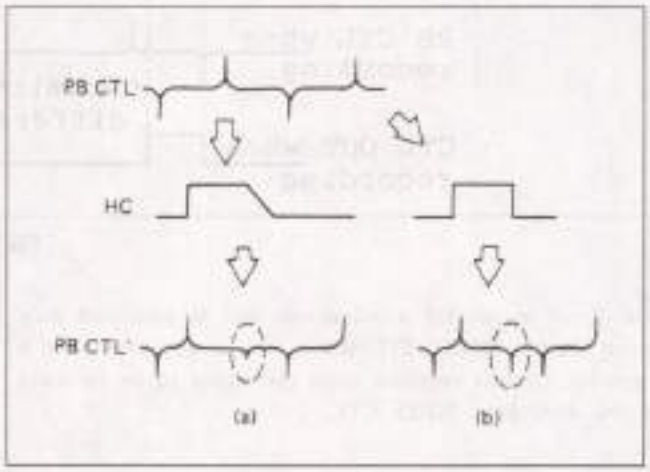


Fig. 3-18

First, since falling of CTL is used by the servo while inserting the INDEX CTL, both INDEX WR and HC CONT are "L" and are sent to the CTL amp in this state. In other sections, the IND WR signal rises (between 5% to 80%) and INDEX CTL will be in write standby state. If the HC CONT signal becomes "H" in this state, Q308 will go ON, current will flow in Pin ㉑, and CTL will be stored.

The HC CONT signal will be "H" between 20% and 60% as shown in Fig. 3-16 and CTL will be stored when rising. The falling part will be smooth as in HC of Fig. 3-18 (a) because of the condenser connected to the collector of Q308. Since the wave form will be like PB CTL' in Fig. 3-18 (b) if in square wave from as shown and will be the cause of servo disturbance because CTL storage is carried out by changing the direction of current flow, sharp changes in current flow are suppressed to minimize the effects on the basic CTL waveform. An IND WR signal is input to Pin ⑦ of IC301 through a CR and this signal is supplied to output CTL with falling required for servo from Pin ⑧ during INDEX CTL recording with the timing shown in Fig. 3-19.

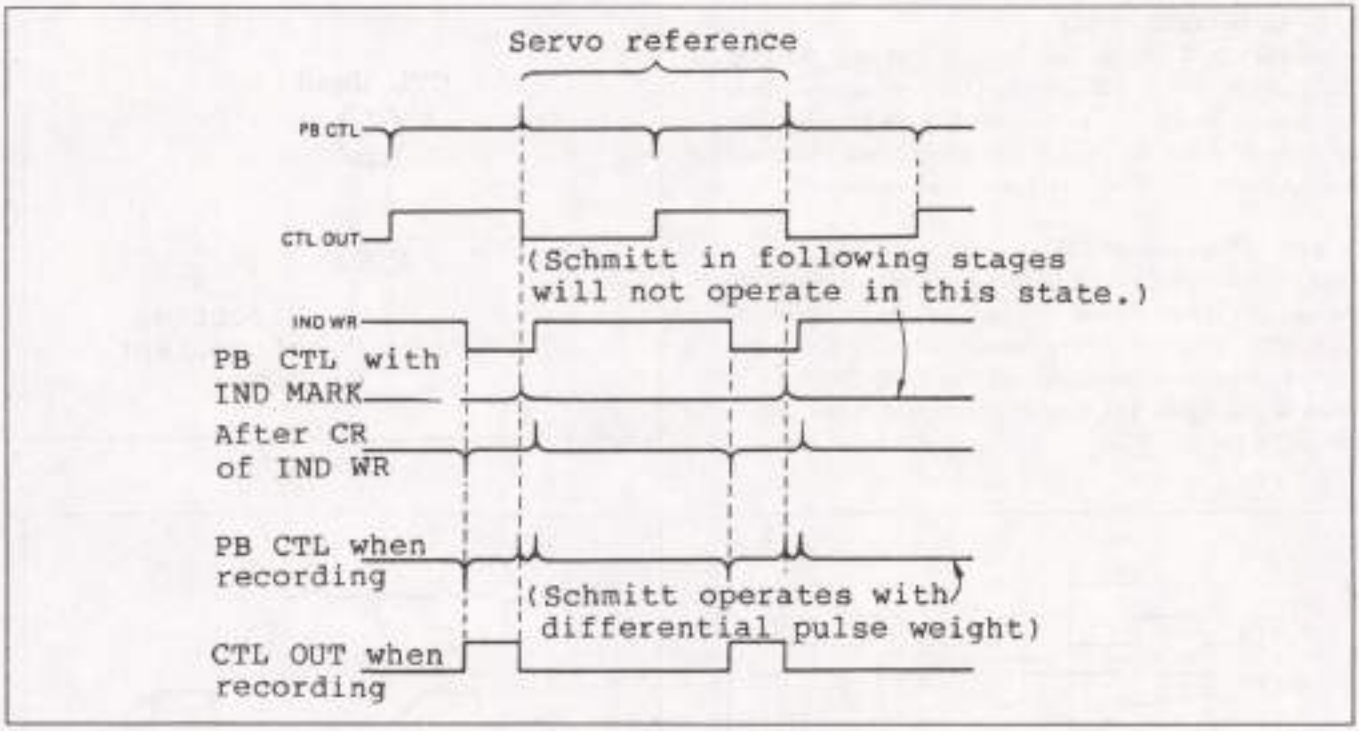


Fig. 3-19

Fig. 3-19 is strictly a waveform that is measured only when storing INDEX CTL and is not a waveform that is recorded. Care is required since the signal to be recorded is the 20% duty INDEX CTL.

3-8-6. INDEX ERASE

The INDEX ERASE function is an opposite operation of IND WR and is to return the 20% duty CTL waveform to the 50% duty NORMAL INDEX. The dynamic chart will be as shown in Fig. 3-20. PB CTL and CTL OUT of Pin ⑧ of IC301 will be output in the waveform shown in Fig. 3-21. By setting to INDEX ERASE mode here, the IND ERA signal will be output in the waveform shown in Fig. 3-20 and it will be in CTL write standby state. If current is causes to flow to the CTL head by the HC CONT signal with the timing shown in Fig. 3-20, CTL will be stored. If we study Fig. 3-20, it will be noted that INDEX ERASE erases the downward slanting CTL at the 20% place in PB CTL and brings it up to the 50% position. As recording is not possible if the falling head current is delayed as in PB WR, the condenser connected to the collector of Q308 is disconnected by the INDEX ERA signal to obtain a sharp change in current of the falling head current. Furthermore, there is no need to record the edge of the HC CONT rising side in IND ER even if rounded since the direction of current flow in the CTL head is the same as the magnetic pattern recorded on the tape.

The state of CTL when erasing INDEX CTL as in the case of PB WR is shown in Fig. 3-21.

PB CTL' and CTL OUT' here are waveforms only seen when erasing. As may be discerned here, falling of the CTL used as servo reference is synchronized throughout during PB, PB WR, PB ERA, REC and during playback after INDEX recording as in the case of PB WR.

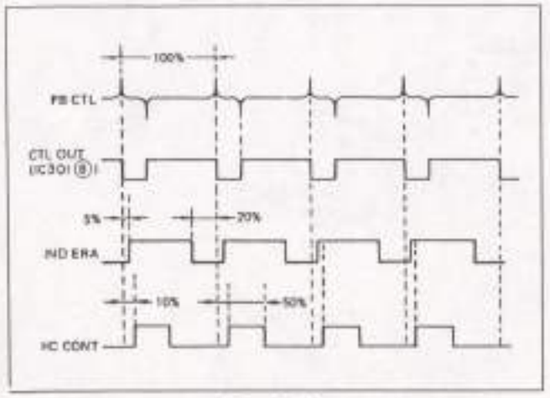


Fig. 3-20

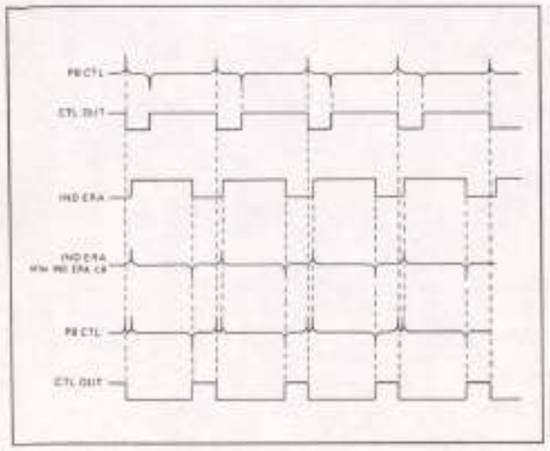


Fig. 3-21

3-8-7. INDEX DETECTOR

The circuit at the upper right of Fig. 3-21 is the INDEX DET circuit that integrates the signal obtained from ID OUT of Pin ④ of IC301 to determine whether it is NORMAL or INDEX CTL, and sends the results to Pin ② of IC010 and compares it with the reference voltage.

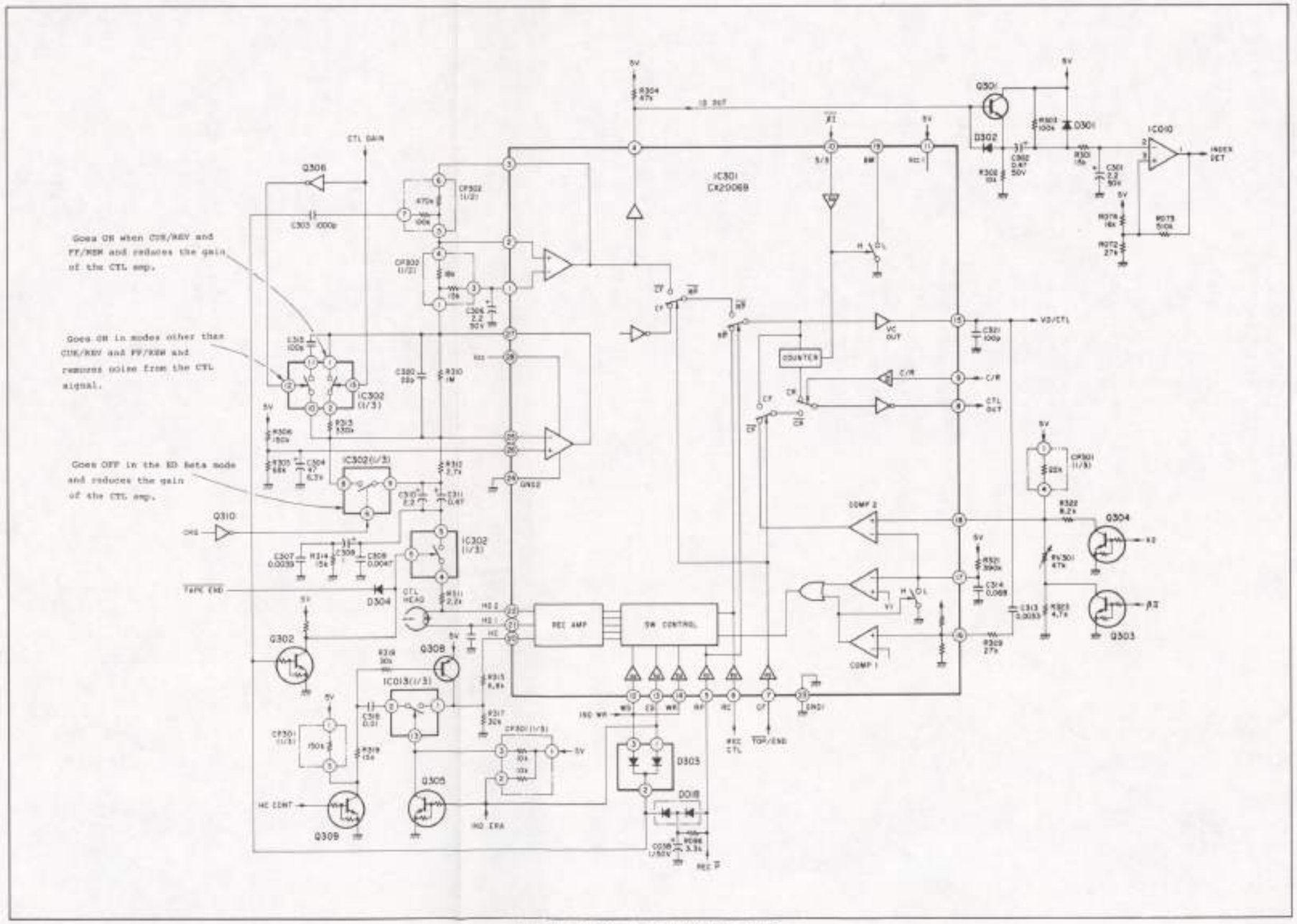


Fig. 3-22 CTL amp and INDEX circuit

4. AUDIO CIRCUIT

4-1. BETA HI-FI RECORDING SYSTEM (AU-38 BOARD)

Compression pre-emphasis is applied by dynamic emphasis of the audio signal, FM modulation is then applied in the modulator, f_1 is then raised to 149.5 kHz by SSB (by lowering f_4) to create f_2 (f_3). f_1 and f_3 are recorded in track A and f_2 and f_4 are recorded in track B.
The FM modulated signal then enters the counter and is compared with the reference 581 Hz signal to form the PLL circuit that outputs the error voltage.

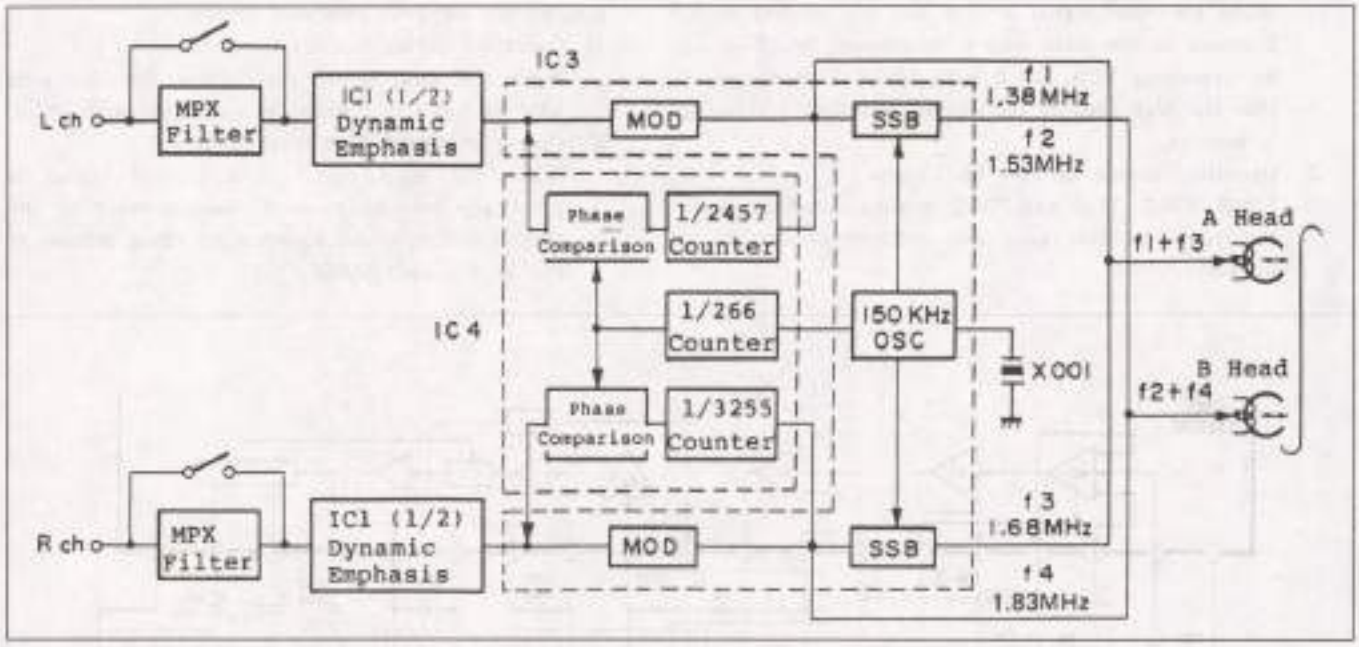


Fig. 4-1

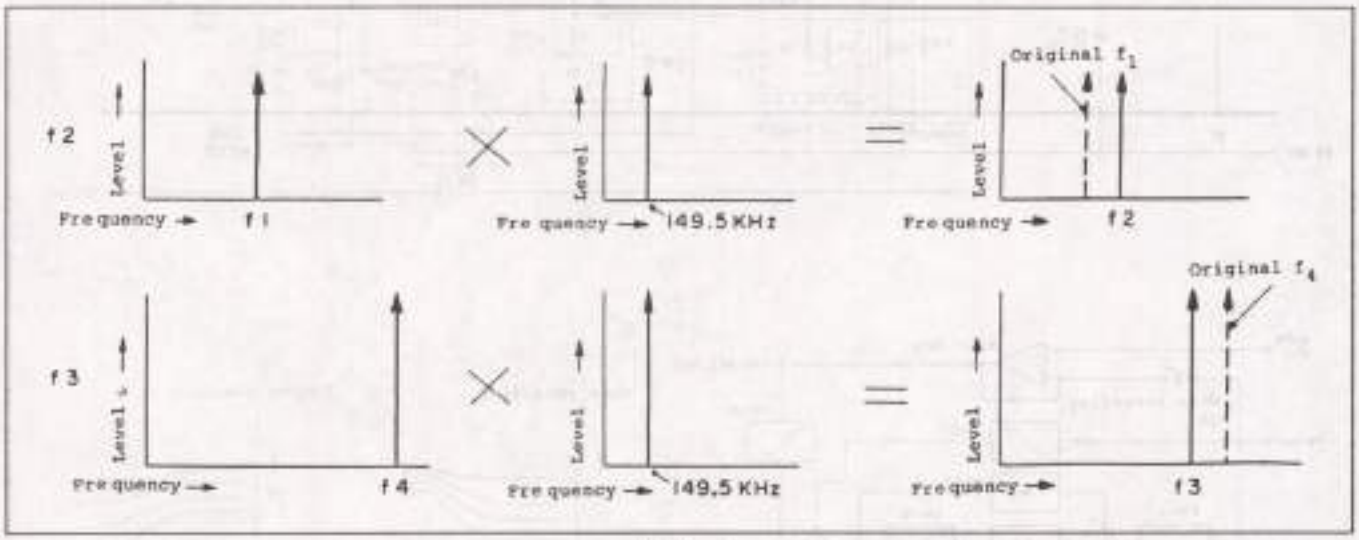


Fig. 4-2

4−1−1. Dynamic Emphasis Circuit

The input signal (MPX FIL output) enters Pins ③ and ㊵ of IC001 and is output from Pins ㉘ and ㉗ during playback and from Pins ㉕ and ㉖ during recording. Dynamic emphasis results in compression and pre-emphasis when recording and expansion and de-emphasis during playback.

(1) REC mode

In the REC mode, the dynamic emphasis circuit operates as the feedback loop of the main amp.

1) Operation during low level input

When the input signal level is low, the amount of feedback of the main amp is determined by EM-I by bypassing VCA EM-Ⅱ with MIGP. This means that the high area of the overall recording system is boosted.

2) Operation during medium level input

EM-Ⅲ, EM-Ⅱ, VCA and EM-I become dominant in the route in this case and emphasis operation increases.

3) Operation during high level input

In the case of high level input signals, EM-I, VCA and EM-Ⅱ are bypassed by MAGP so the amount of feedback of the main amp will no longer be concerned with EM-I and EM-Ⅱ (EM-Ⅲ serves to correct the f characteristics of MAGP) and the f characteristics become flat in the overall recording system.

(2) PB mode

In the PB mode, the signal is output from the main amp through the dynamic emphasis circuit.

1) Operation during low level input

When the input signal level is low, the high area level by EM-I is lowered by bypassing with MIGP.

2) Operation during high level input

When the input signal level is high, there is practically no change in f characterisitcs of the overall system similar to when recording because of the bypass with MAGP.

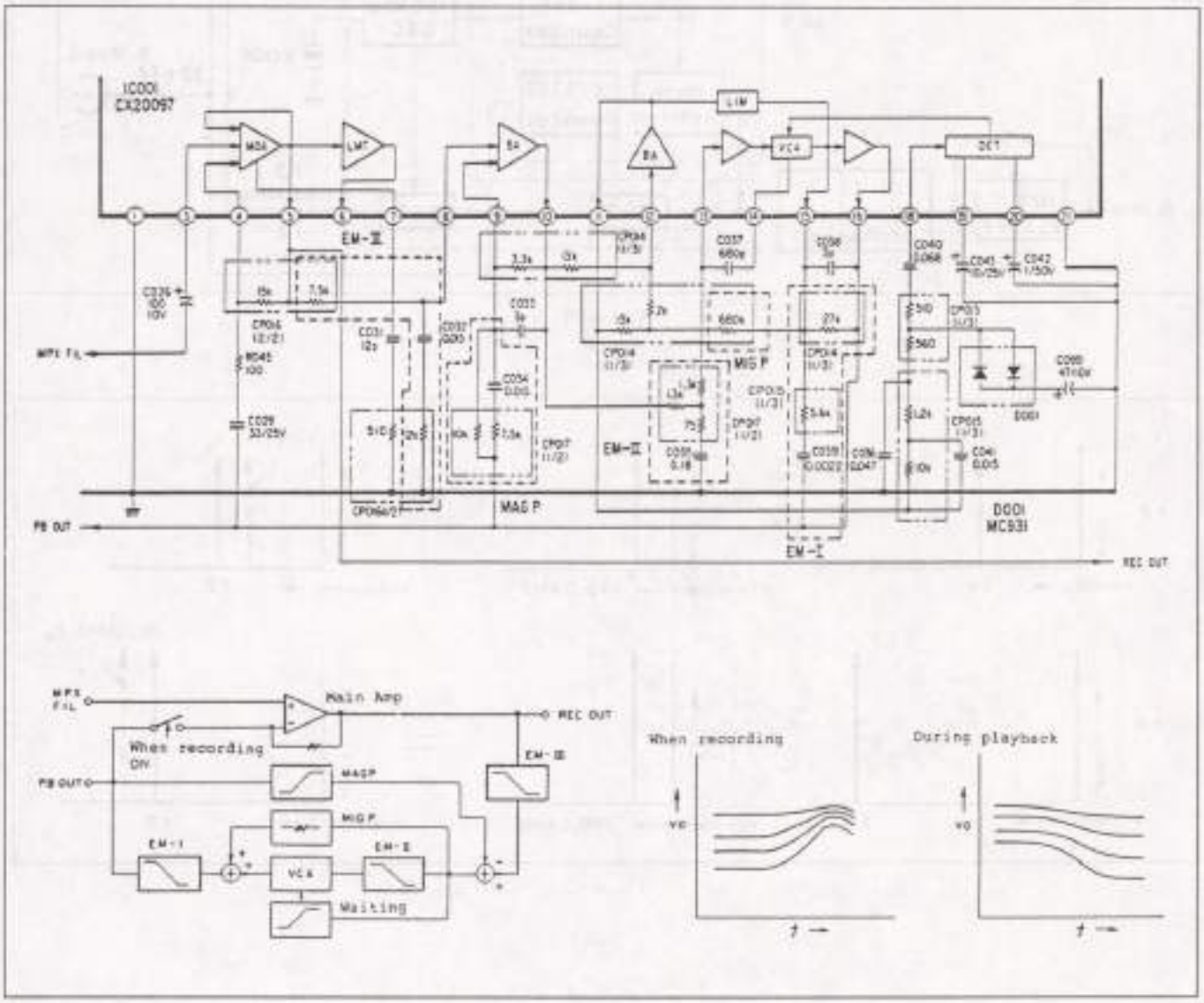


Fig. 4−3

4-1-2. PLL Circuit

When REC, the output signal of the dynamic emphasis circuit is input to Pins ③ and ㊽ of IC003 and is output from Pins ⑥ and ㊸ for use as a PLL loop after being FM modulated by MOD1 and MOD2.

The signal output from Pins ⑥ and ㊸ of IC003 is input to Pins ③ and ⑬ of PLL IC004. A 150 kHz signal from Pin ㊽ of IC003 (150 kHz OSC output) is input to Pin ⑬ of IC004. Phase comparison is conducted on the signals input to IC004 and the error voltage is output from Pins ④ and ⑪ of IC004 and is input to the signal input of IC003.

The LPF of the internal switch of IC004 is bypassed to hasten startup of the loop when power is turned on.

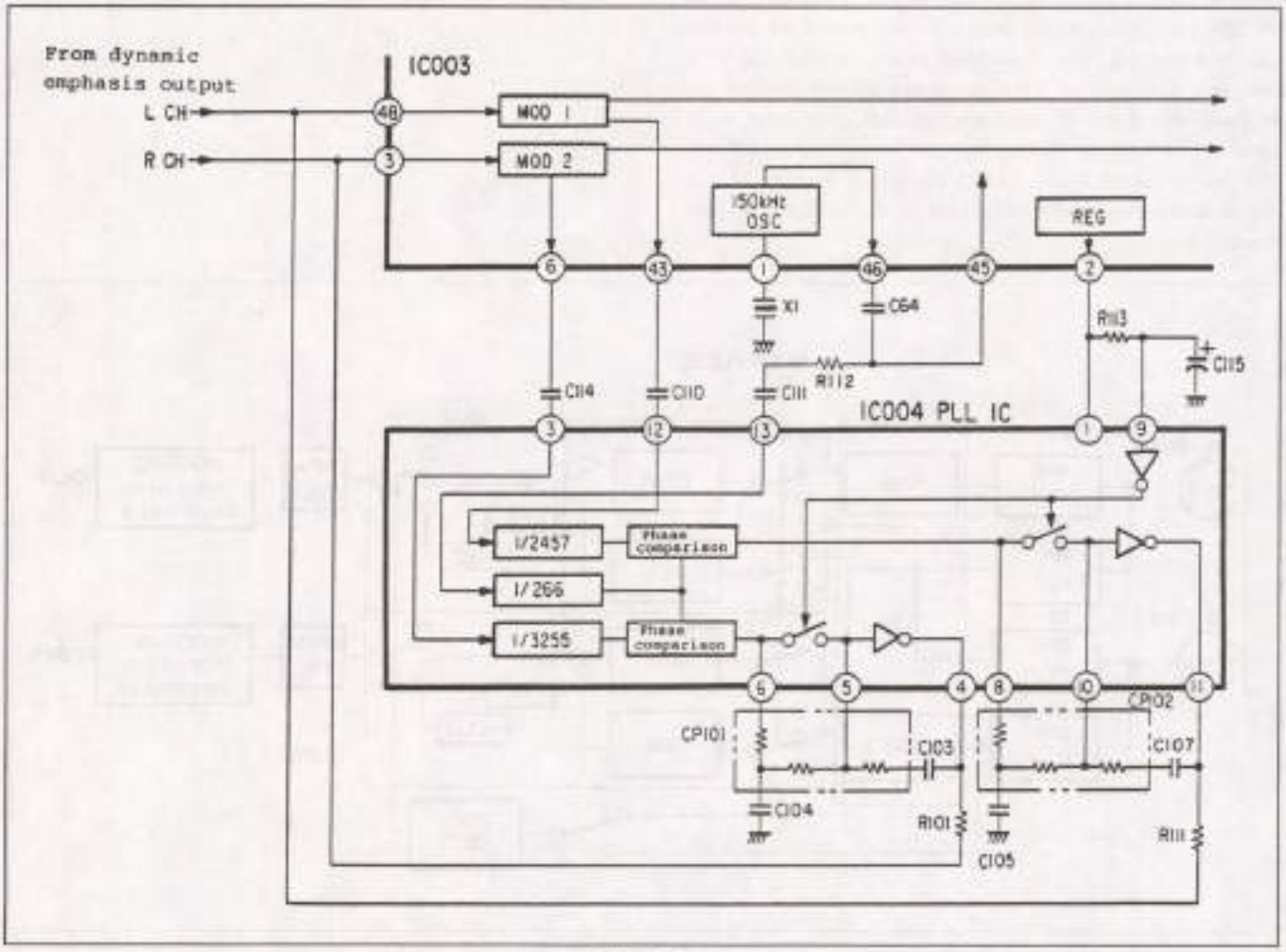


Fig. 4-4

4-2. BETA HI-FI PLAYBACK SYSTEM (AU-38 BOARD)

Frequency f_1 modulated by the audio frequency of the Lch and frequency f_3 modulated by the audio frequency of the Rch are recorded on track A. Frequency f_2 modulated by the audio frequency of the Lch and frequency f_4 modulated by the audio frequency of the Rch are recorded on track B.

Frequency f_1 is converted to f_2 by SSB and f_4 is converted to f_3 by SSB and the signals are input to each demodulator. Switcing of track A and track B is performed by RF SW Pulses in this case.

The FM frequency is demodulated by the demodulator and becomes audio signals. When the carrier frequency drops out, the next hold circuit holds it and serves to prevent noise and blurring. The signal then passes through the MPX filter and is output as low frequencies after expansion de-emphasis by dynamic emphasis according to the input signal.

This unit employs the 4 DEMO system. A feature of this system is low noise during playback of high frequency pure tones.

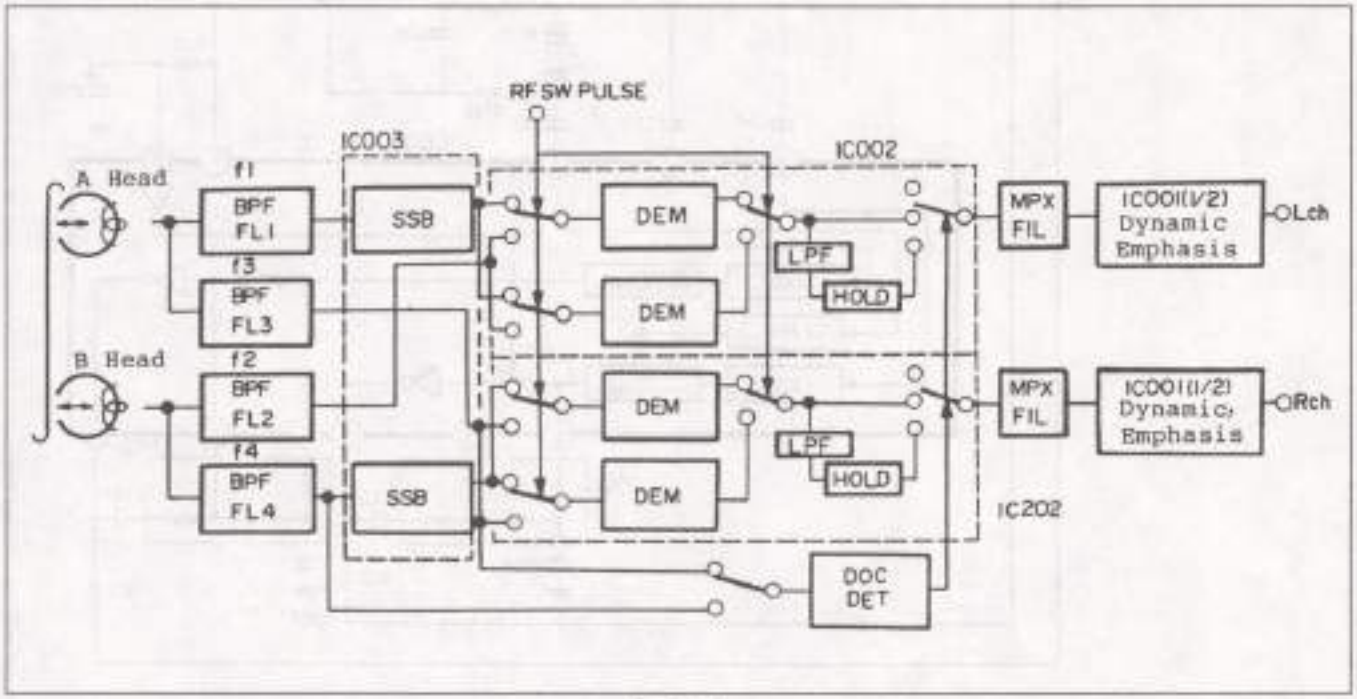


Fig. 4-5

4-2-1. AF-MUTE Circuit

If there is a dropout, a signal from DOC DET of IC003 enters Pin ⑥ of IC002 (IC202) and operates SW4 with SW CONT to cut audio signals received. Sets to AF-MUTE state during hold or when extended time is required.

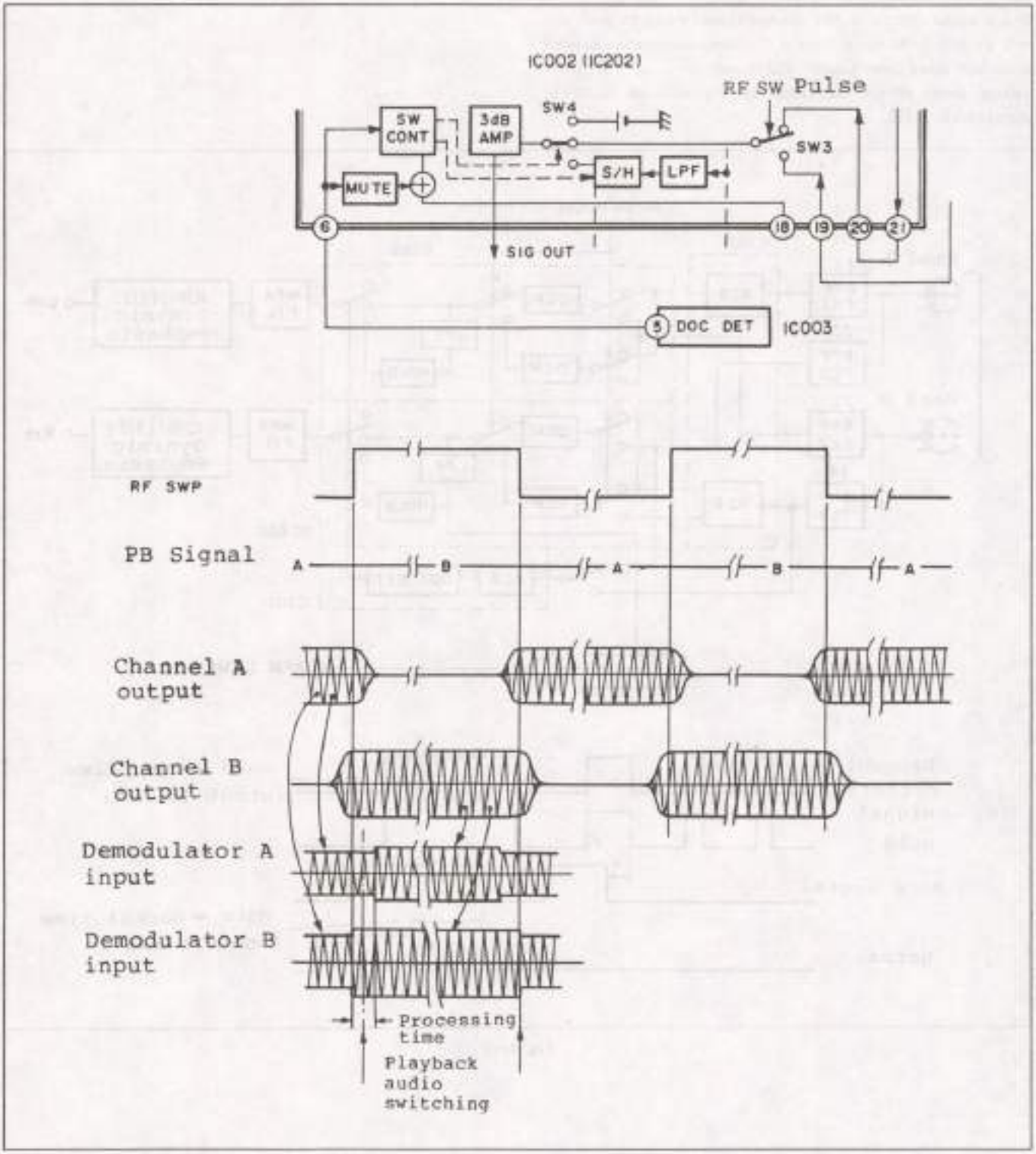


Fig. 4-6 Switching diagram

4-2-2. Dropout and AF Mode

If a dropout occurs in the AFM signal, it will change over to the following three states.

(1) Hold

(2) AFM mute

(3) Normal track

If a dropout occurs, it will change immediately to hold and will go into AFM mute state if the dropout extends beyond a certain fixed time (about 100 μsec).

Levels above 50 kHz are read by AF DET of IC202 to discriminate AFM.

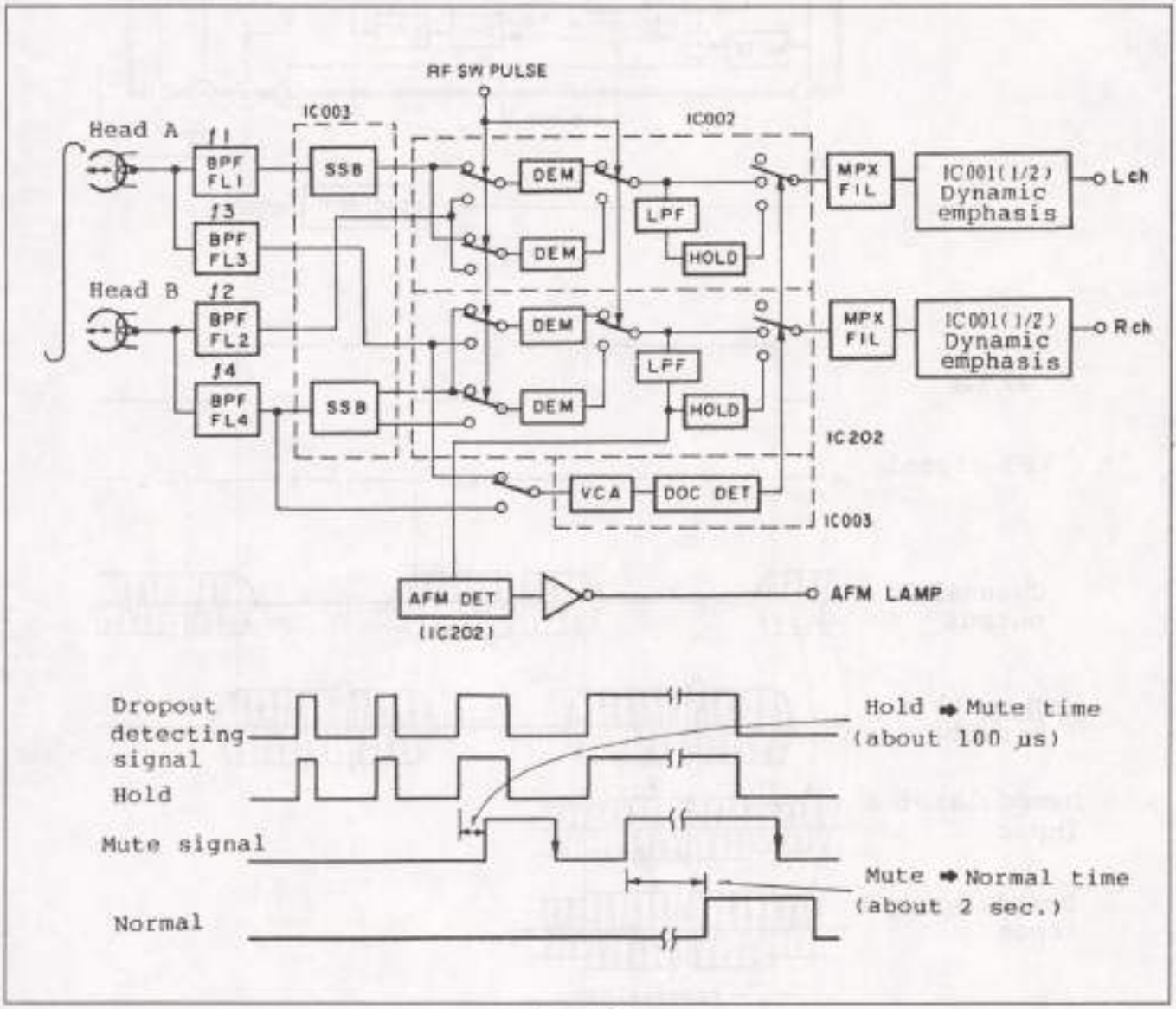


Fig. 4-7

4-3. MPX FILTER SWITCHING CIRCUIT (AU-38 BOARD)

If the MPX terminal is set to "H" to remove unwanted noise in the audio signal, Q151 (351) – Q153 (353) of the AU-38 board go ON and operate as the 15 kHz LPF. They operates as a 20 kHz LPF when the MPX terminal is "L" or during playback.

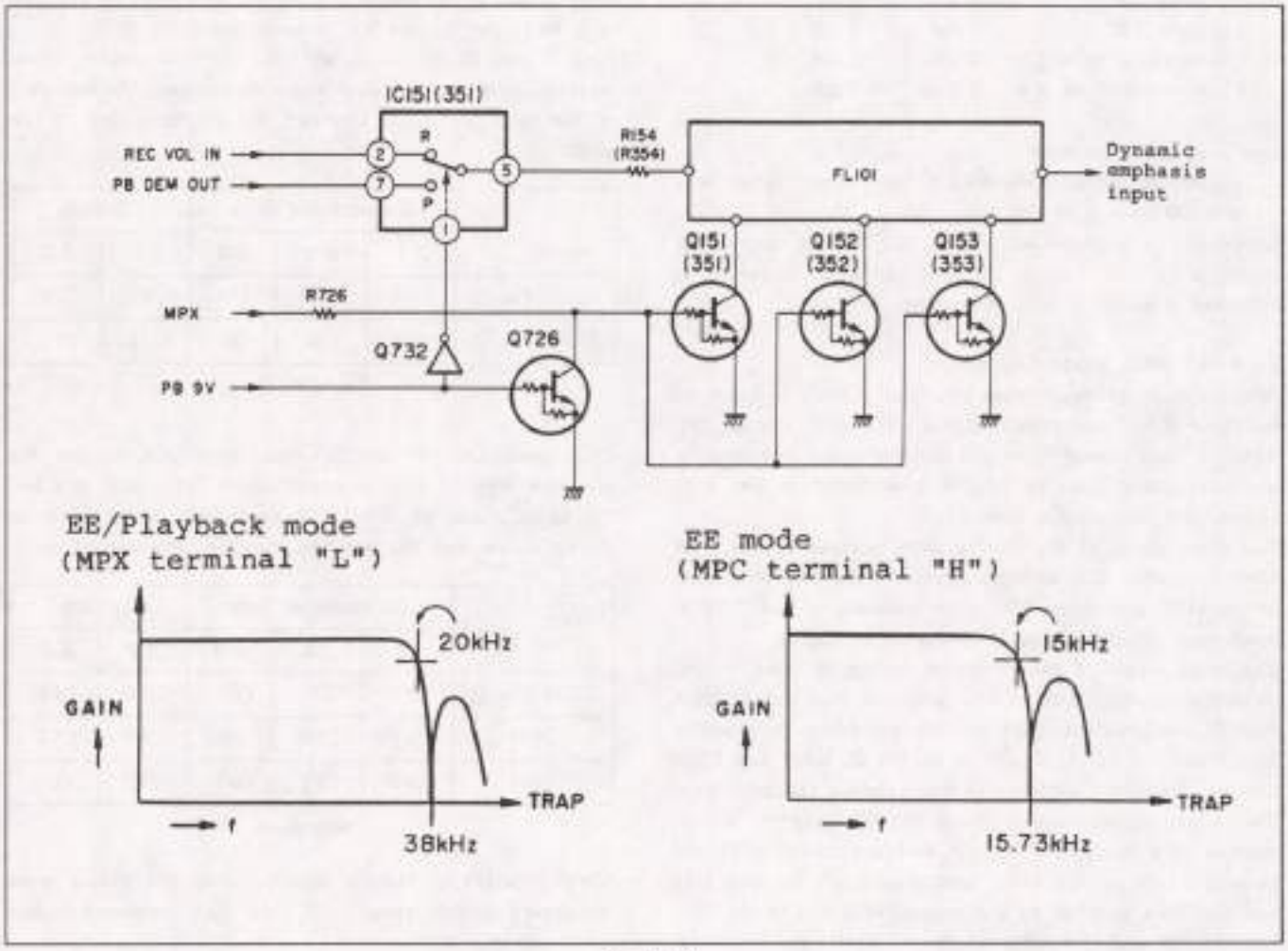


Fig. 4-8

4-4. NORMAL AUDIO CIRCUIT (VE BOARD)

The normal audio circuit is configured principally of the VE board and IC901, PB/EE switching in normal audio is carried out by IC802 in the AU-38 board.

By using a metal tape, the frequency characteristics of this machine were improved as follows.

High area characteristics

ED Beta β II	100 kHz	−3 dB
ED Beta β III	7 kH	−3 dB
Conventional Beta β II	8 kHz	−3 dB
Conventional Beta β III	5 kHz	−3 dB

Low area characteristics

Regardless of the mode, both ED and conventional Beta are 100 Hz −2 to −3 dB.

Compared to conventional Beta, S/N has also been improved by 1 to 2 dB in ED Beta and sense of feeling is improved from an audible viewpoint.

4-4-1. REC Mode Operation

The audio signal input from Pin ④ of CN904 is input to Pin ㉘ of IC901 and passes through the AGC circuit. The signal is then output from Pin ㉙ after being amplified in the line output amplifier and is then input to the AGC system and recording system.

The audio signal of the AGC system is input to Pin ㉗ of IC901 and, after AGC detection, becomes the control voltage of the AGC attenuator. The time constant of the AGC is determined by the C and R of Pin ㉖ of IC901.

The audio signal of the recording system is input to the recording equalizer amp of Pin ㉔ and is then output from Pin ㉕. The characteristics of this recording equalizer is determined by the L, C and R of Pin ㉓. Q902 and Q903 are the changeover switches of the equalizer characteristics. The audio signals output from Pin ㉕ separate into L channel and R channel signals and are mixed with the recording bias current after passing through the bias trap and are then supplied to the respective audio heads.

Q902, Q903 and Pins ㉑ and ㉒ of IC901 go ON/OFF corresponding to the mode as shown in the table below.

	Conventional Beta		ED Beta	
	β II	β III	β II	β III
Q902	OFF	OFF	OFF	ON
Q903	OFF	OFF	ON	OFF
IC901 Pin ㉑	OFF	ON	OFF	OFF
IC901 Pin ㉒	ON	OFF	OFF	OFF

Table 4-1

4-4-2. Playback Mode Operation

The audio signal reproduced in the Lch audio head is input to is input to Pin ⑬ of IC901 and is output from Pin ⑪ after being amplified in the PB EQ AMP. C906, 909 and 912 use the resonance with the L components of the head and improve high frequency characteristics. The audio signal output from Pin ⑧ is input to Pin ㉚ after its playback level is set by RV901 and, after passing through the line amp, is output to the AU-38 board from Pin ㉛.

Pins ⑦ and ⑫ of IC901 go ON/OFF as shown below corresponding to the mode and changes over the resonant of the head and C906, 909 and 912 corresponding to the mode.

	Conventional Beta			ED Beta	
	β I	β II	β III	β II	β III
IC901 Pin ⑦	OFF	OFF	ON	OFF	OFF
IC901 Pin ⑫	OFF	ON	ON	OFF	OFF

Table 4-2

Q905 goes ON in the ED Beta mode and adjusts the playback level to that of conventional Beta. Q901, 904 and Pin ⑪ of IC901 go ON/OFF according to the mode as shown below and changes the equalizer characteristics.

	Conventional Beta			ED Beta	
	β I	β II	β III	β II	β III
IC901 Pin ⑪	OFF	ON	OFF	OFF	OFF
Q901	OFF	OFF	ON	OFF	OFF
Q904	OFF	OFF	OFF	OFF	ON

Table 4-3

Q906 goes ON in Picture Search during the editing work or during double speed and cuts high frequency noises (−20 dB at 5 kHz).

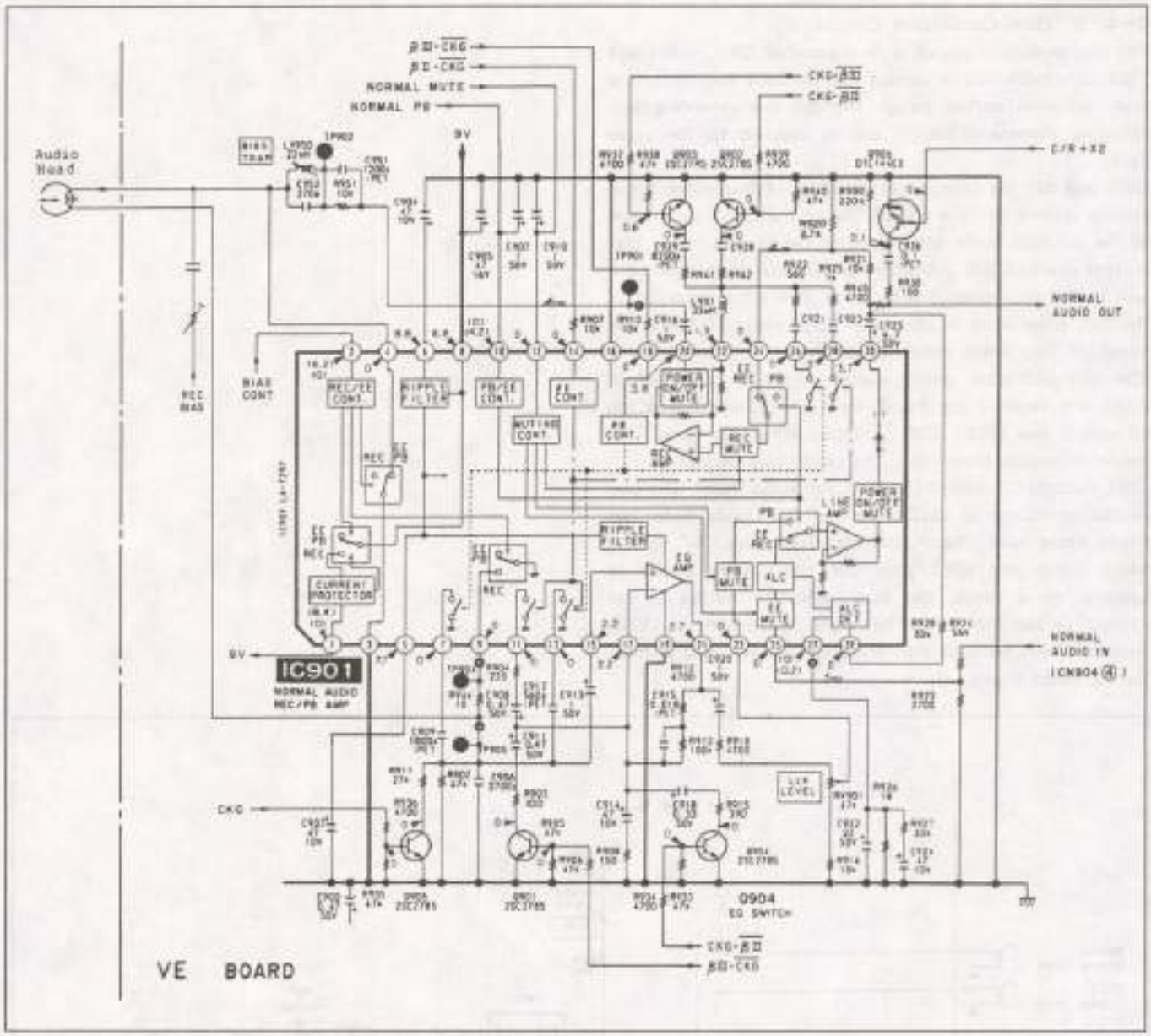

NORMAL MUTE
NORMAL PB
Audio Head
9V
NORMAL AUDIO OUT
BIAS CONT
REC BIAS
IC901
NORMAL AUDIO REC/PB AMP
NORMAL AUDIO IN (CN804 ④)
CKG
0904
EQ SWITCH
VE BOARD

Fig. 4-9

4-4-3. Bias Oscillation Circuit

The bias oscillation circuit is configured of Q801 – 804 and T801. Bias oscillation is carried out by Q802 and T801. The bias oscillation output passes through the recording bias adjusting element (RV802) and is supplied to the audio heads.

Q803 and 804 are changeover switches of bias current and erasing current and are turned ON by the CKG signal when in the ED Beta mode and increases the current. (The bias current is about 500 μA when in ED Beta mode, about 310 μA in the conventional Beta mode. The voltage applied to the full erase head is about 50 Vp-p when ED Beta and about 35 Vp-p when conventional Beta.)

The bias oscillation power supply switch is contained in IC901 and becomes the Pin ⑭ input, Pin ① output and Pin ② control bias (BIAS CONT) input. When Pin ② is "H", power is output from Pin ① to cause bias oscillation.

Q801 controls the switch (RY801) for audio insert. The bias oscillation output is applied to the Full Erase head and Auido Erase head. The A. INS signal becomes "H" during audio insert and Q801 goes ON and causes RY801 to operate. As a result, the bias oscillation output is not applied to the Full Erase head but is applied to LV801 instead. LV801 becomes the recording bias adjusting element during audio insert.

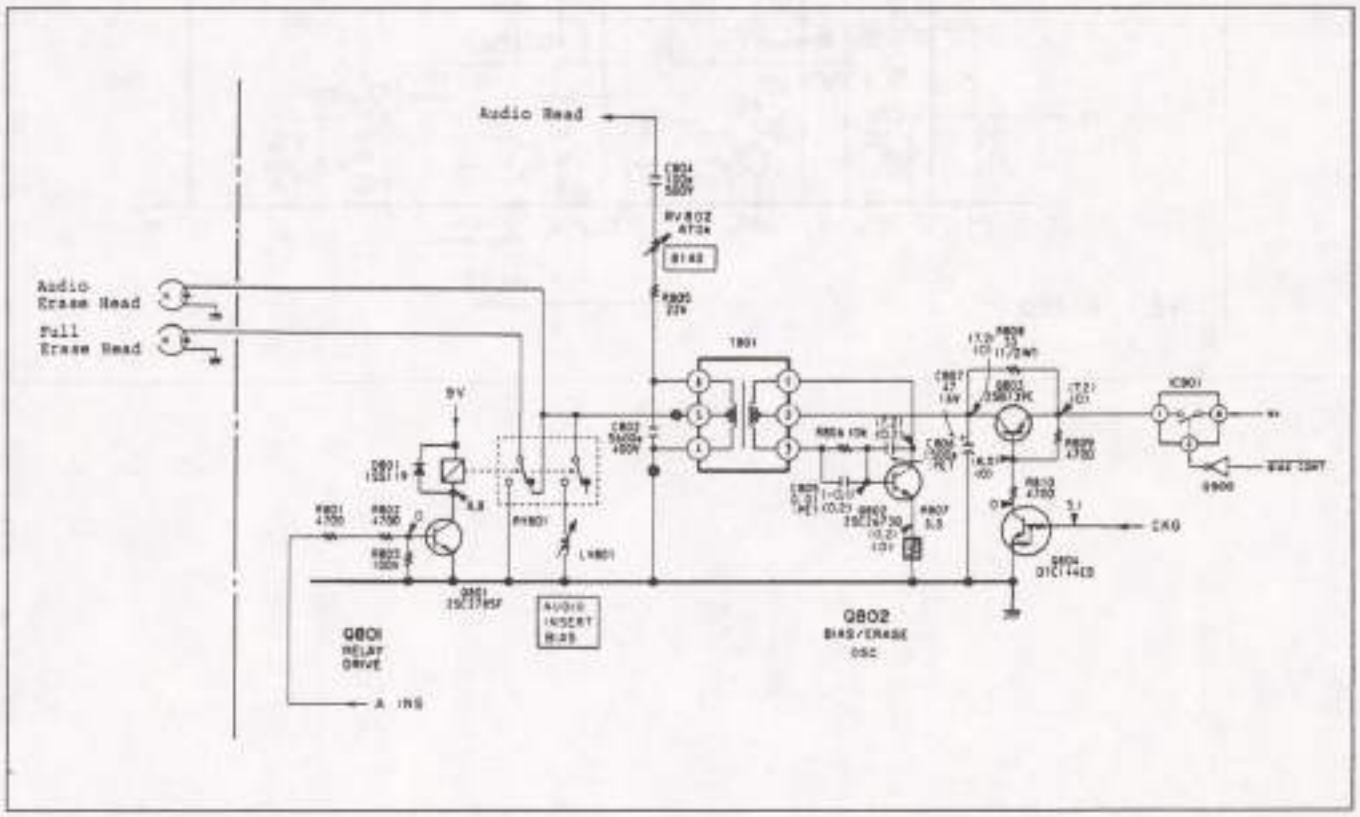


Fig. 4-10

4-5. PERIPHERAL AUDIO CIRCUITS

4-5-1. Audio Input Switching Circuit (AU-38 Board)

The four inputs TUNER/SIMUL CAST/LINE 1/LINE 2 are available as audio inputs.

TUNER : The tuner audio signals are input to both β-HIFI and normal audio circuits.

SIMUL CAST : Line 1 audio is input to the β-HIFI circuit and the tuner audio is input to the normal audio circuit.

LINE 1 : Line 1 audio (pin jack on back of set) is input to both β-HIFI and normal audio circuits.

LINE 2 : Line 2 audio (pin jack on the front of the set) is input to both β-HIFI and audio circuits.

Furthermore, since the normal audio circuit is for monaural recording, the Lch and Rch signals are mixed in the output of IC505 and is output to the VE-1 board after passing through the tuner audio switching circuit in IC804 and the MIC audio switching circuit in IC801.

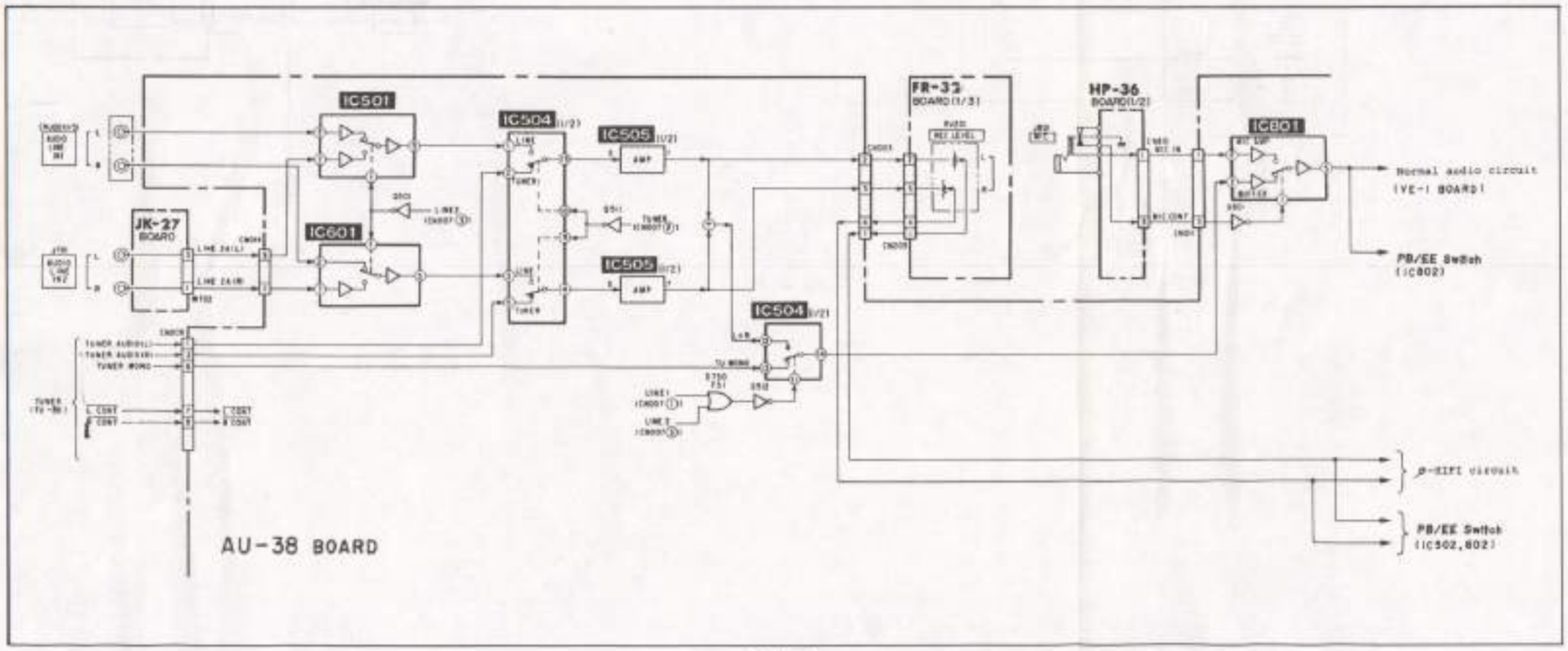


Fig.4-11

4-5-2. Audio Output Switching Circuit

The β-HIFI audio signal passes through the PB/EE switch IC502 and 602, β-HIFI/MIX/NORMAL switching circuit IC506, and the STEREO/Lch/Rch switching circuit IC507 and 607 and is output to the audio output terminal.

The normal audio signal passes through the PB/EE switch IC802, β-HIFI/MIX/NORMAL switching circuit and the STEREO/Lch/Rch switcing circuit IC507 and 607 and is output to the audio output terminal.

Although the PB/EE switch IC502, 602, 802 normally selects the output signal of the β-HIFI circuit or the normal audio circuit, it selects the EE signal output of the input switching circuit during playback only while the EE button is depressed. The β-HIFI/MIX/NORMAL switching circuit IC506 is controlled by the $\overline{\text{NORMAL}}$ signal and $\overline{\beta\text{-HIFI}}$ signal and changes over the signal as shown in the table below according to the position of the AUDIO MONITOR switch. If a tape without β-HIFI recording is played back, the $\overline{\text{NORMAL}}$ signal is forced to "L" by the logic of Q709, 710, 712 and the normal audio circuit output signal is selected.

AUDIO MONITOR Switch Position	HIFI	MIX	NORMAL
$\overline{\beta\text{-HIFI}}$	L	H	H
$\overline{\text{NORMAL}}$	H	H	L
Audio Output	β-HIFI	β-HIFI/ NORMAL mix	NORMAL

Table 4-4

The STEREO/Lch/Rch switching circuits IC507 and 607 are controlled respectively by the $\overline{\text{L CONT}}$ and $\overline{\text{R CONT}}$ signals and the output signal is changed over as shown in the table below each time the L/R button is pressed during playback, audio insert.

In other cases, it will be in STEREO mode and both signals will be "L".

Fluorescent character display tube indication	STEREO, or no indication	L	R
$\overline{\text{L CONT}}$	L	H	L
$\overline{\text{R CONT}}$	L	L	H
Lch audio output	Lch	Lch	Rch
Rch audio output	Rch		

Table 4-5

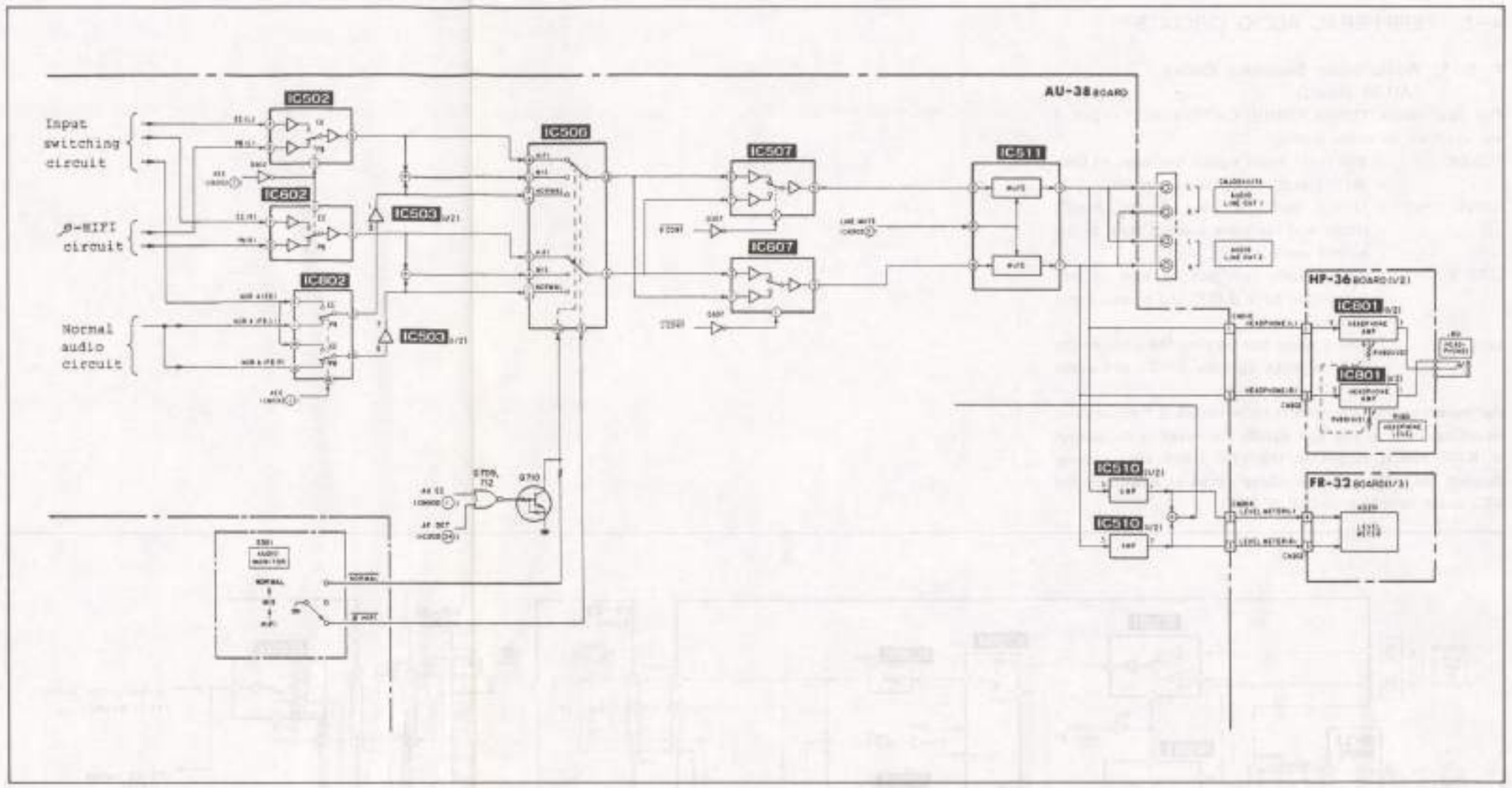


Fig. 4-12

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